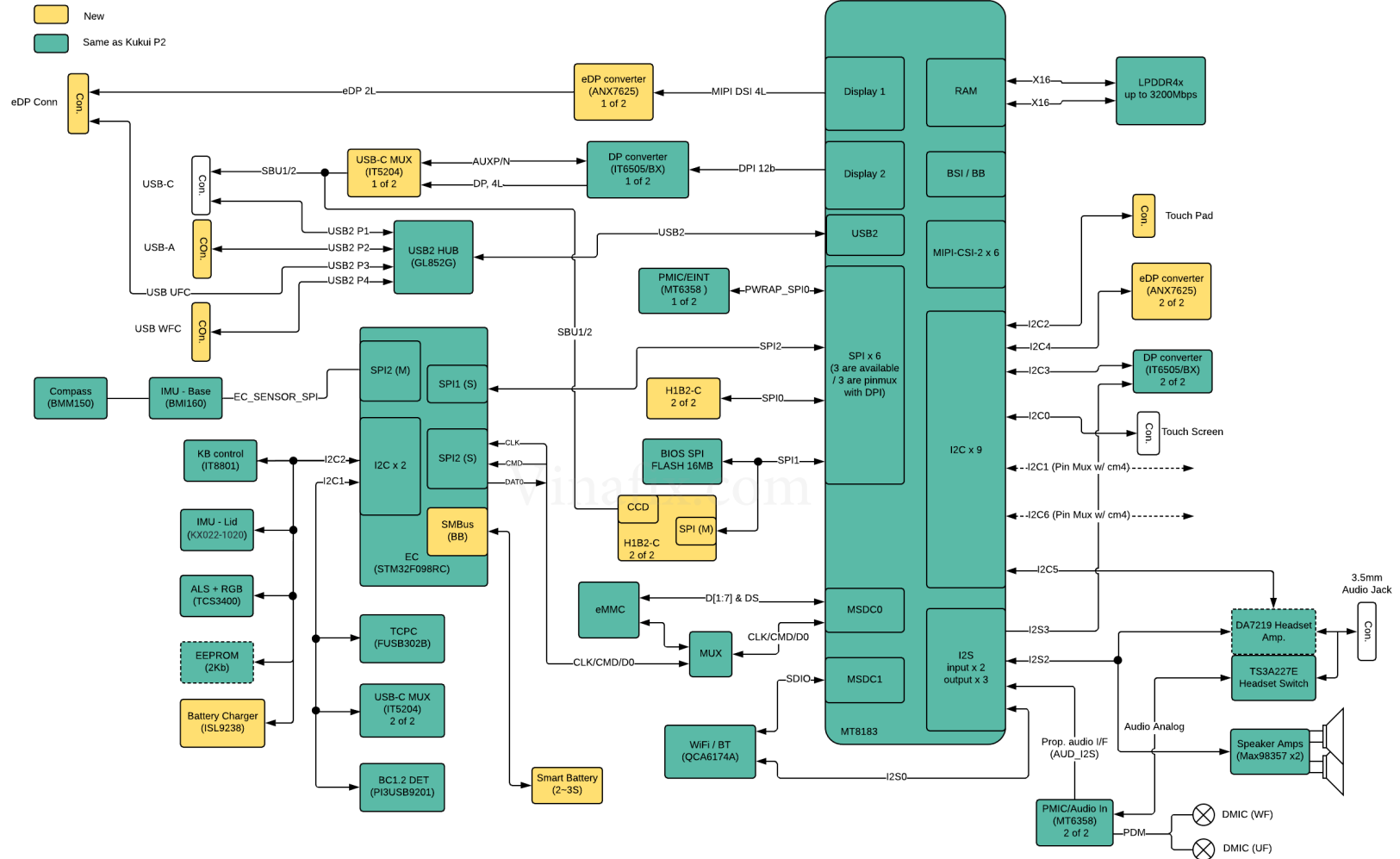


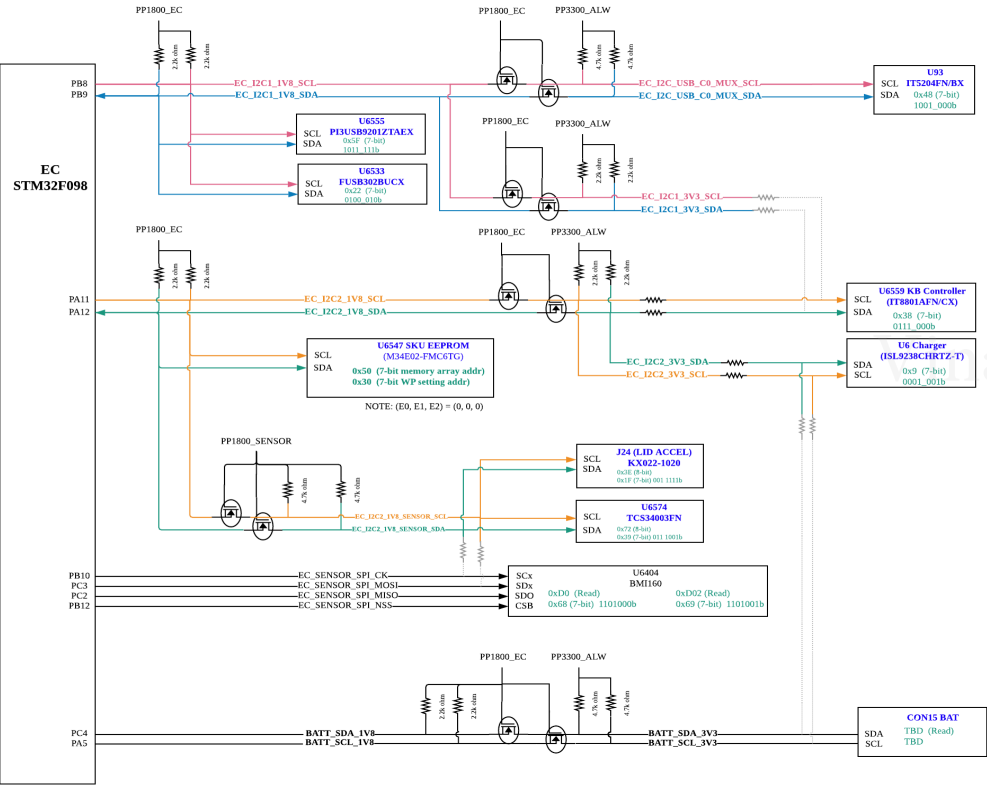
Jacuzzi Proto
MT8183 Chromebook Convertible
2019-12-16



Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

EC_I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)	Note
I2C-1	IT5204FN/BX			0x90 (8-bit) ; 0x48 (7-bit)	
	PI3USB9201ZTAEX			0xBE (Read)	
	FUSB302BUCX			0x44 (Read)	
	IT8801BFN/CX			0x70 (8-bit) 0111_000b	Default NC
I2C-2	IT8801BFN/CX			0x70 (8-bit) 0111_000b	
	ISL9238CHRTZ-T			0x12 (8-bit) 0001_001b	
	BATTERY			0x?? (Read) ???_??b	
	KX022-1020			0x3E (8-bit) ; 0x1F (7-bit) 001 1111b	
	TCS34003FN			0x72 (8-bit) ; 0x39 (7-bit) 011 1001b	
	M34E02-FMC6TG			Memory area select code: 0xa0, PSWP: 0x60	
	BMI160			0xD0 (Read) 0x68 (7-bit) 1101000b 0xD02 (Read) 0x69 (7-bit) 1101001b	Default NC

Jacuzzi EC I2C Block Diagram



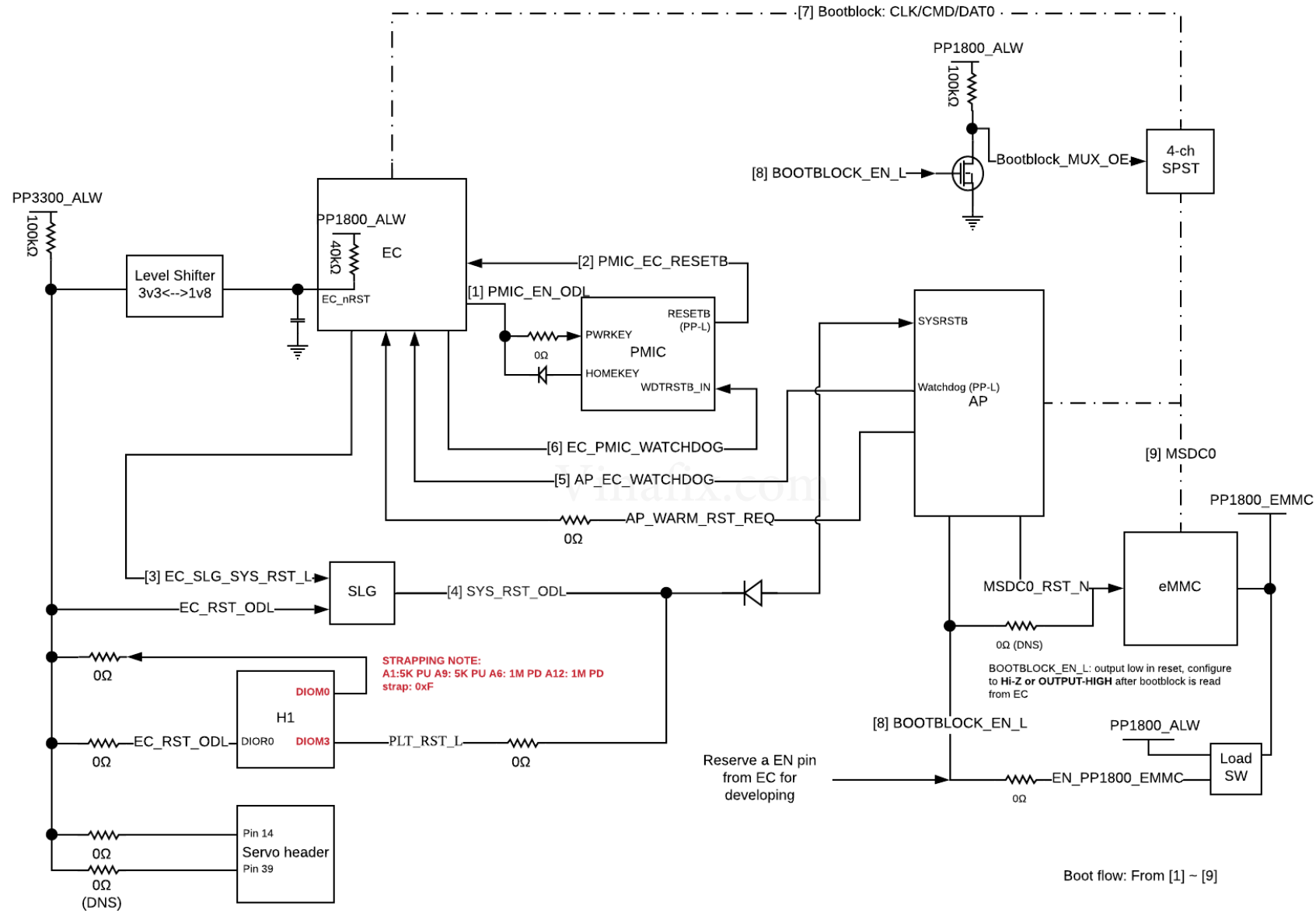
I2C	AP, SCP	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)	Note
I2C-0	AP	CTP		Yes.	0X10	
I2C-1 (I3C)	TBD	-		Yes.	-	
		-		Yes.	-	
I2C-2 (I3C)	AP	Track Pad		Yes.		
I2C-3	AP	IT6505		Yes.	0x5C	
I2C-4 (I3C)	AP	ANX7625BN-AC-R		Yes.		
I2C-5	AP	DA7219		Yes.	0x1A	Default NC
		TS3A227EYFFR		Yes.	0x3B	
I2C-6	TBD	-		Yes.	-	

I2S	Device	Function
I2S2_MCK I2S2_BCK I2S2_LRCK I2S2_DI I2S3_DO	DA7219	Earphone
I2S5_BCK I2S5_LRCK I2S0_DI I2S5_DO	MAX98357AEWL+T	Speaker AMP
I2S3_TDM_BCK I2S3_TDM_LRCK I2S3_TDM_D0 I2S3_TDM_D1 I2S3_TDM_D2 I2S3_TDM_D3	U69H025.XX	Wifi Module BT
	IT6505	DPI to DP bridge audio

SPI		
Net Name	Master	Slave
AP_SPI_FLASH_CS_L AP_SPI_FLASH_CLK AP_SPI_FLASH_MOSI AP_SPI_FLASH_MISO	AP	NOR FLASH
SPI_AP_EC_CS_L SPI_AP_EC_CLK SPI_AP_EC_MOSI SPI_AP_EC_MISO	AP	EC
DEBUG_SPI_FLASH_CS_L DEBUG_SPI_FLASH_CLK DEBUG_SPI_FLASH_MOSI DEBUG_SPI_FLASH_MISO	H1 or Servo	NOR FLASH

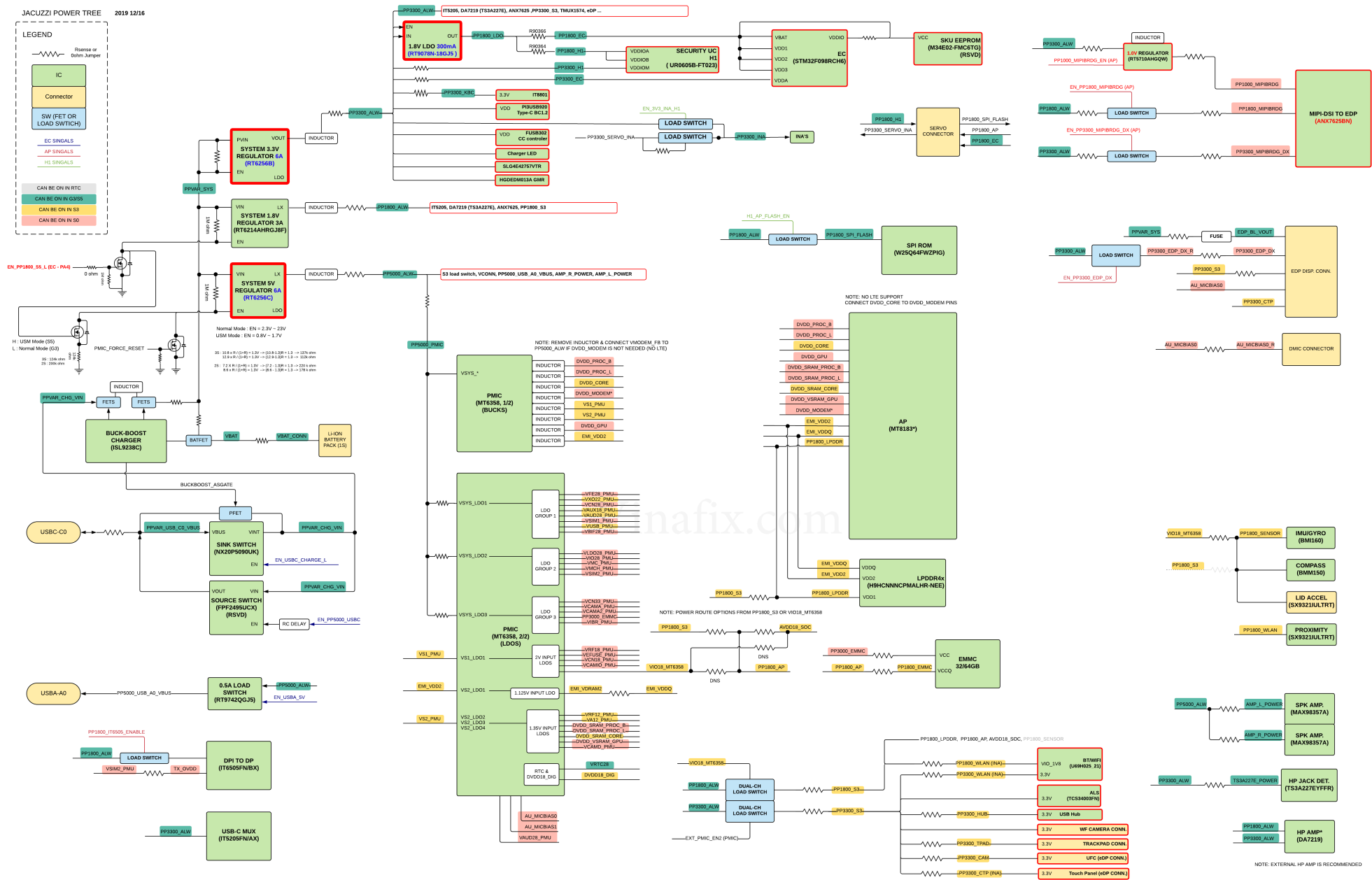
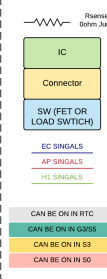
BOM value option	
AL58	Ambient Light Sensor (*default non)
Q989	CMR Sensor (*default non, Q98 is on SUB-SOARD)
2389	2nd camera (*default non)
8208	E-compass (*default non)

Reset Map
Ver2.3

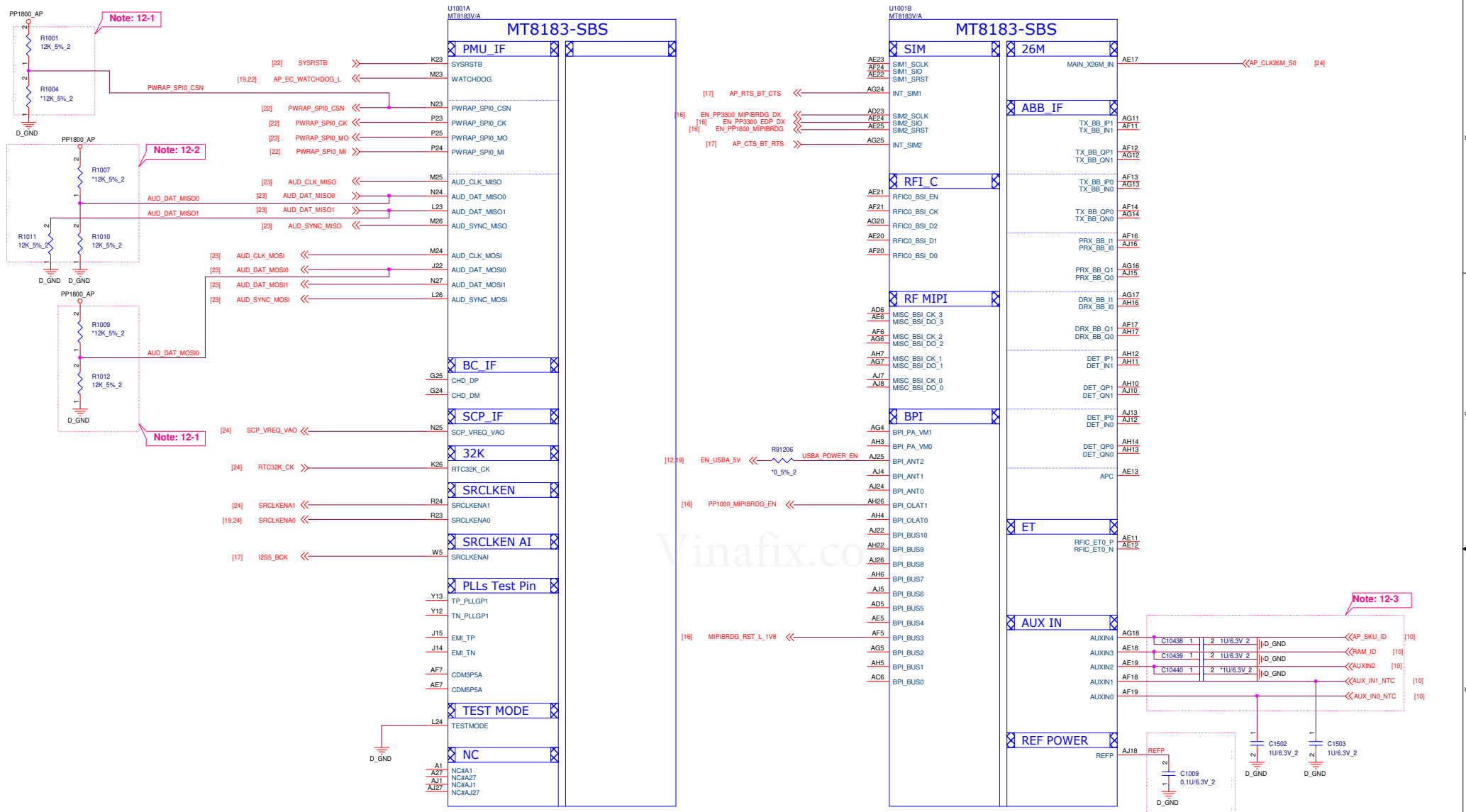


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LEGEND



NOTE: EXTERNAL HP AMP IS RECOMMENDED



Schematic design notice of "BB_1" page.

Note 12-1: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP_JTAG	IO_JTAG
HI	LO	N/A	N/A
HI	HI	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	N/A
LO	LO	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	DPI_11/DPI_HSYNC/DPI_VSYNC/DPI_DE/ DPI_CK/DPI_D8/DPI_D9
LO	HI	MSDC1_CLK/CMD/ DAT0/DAT1/DAT2	N/A

Note 12-2: "AUD_DAT_MISO0" is bootstrap pin to enable serial JTAG output over USB2.0 interface or not.
When "AUD_DAT_MISO0" is pulled to high in system start up and then USB2.0 interface will be switched into serial JTAG mode.

"AUD_DAT_MISO1" is bootstrap pin to select system booting up from eMMC or UFS device.

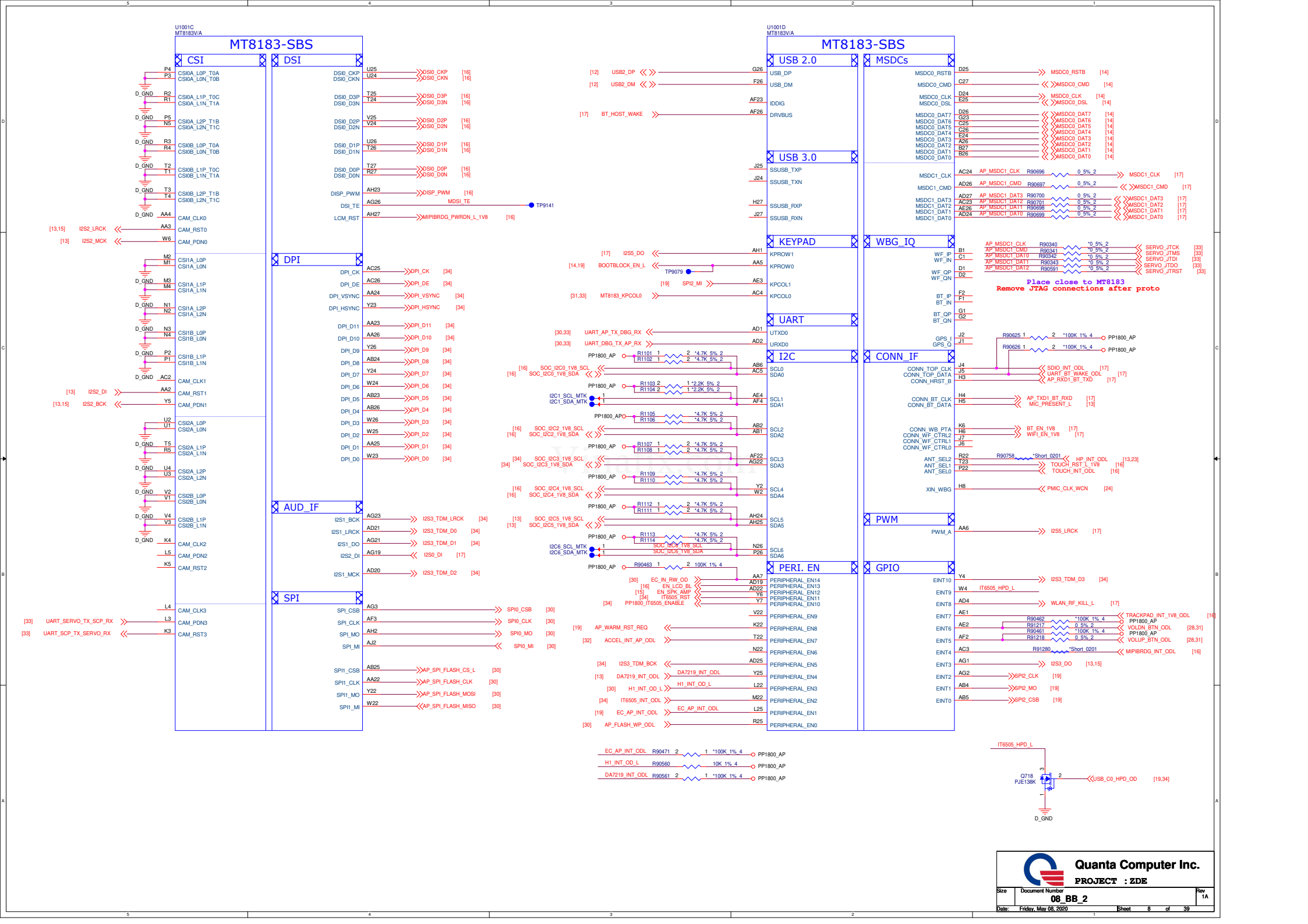
AUD_DAT_MISO1	Boot device
LO	eMMC
HI	UFS

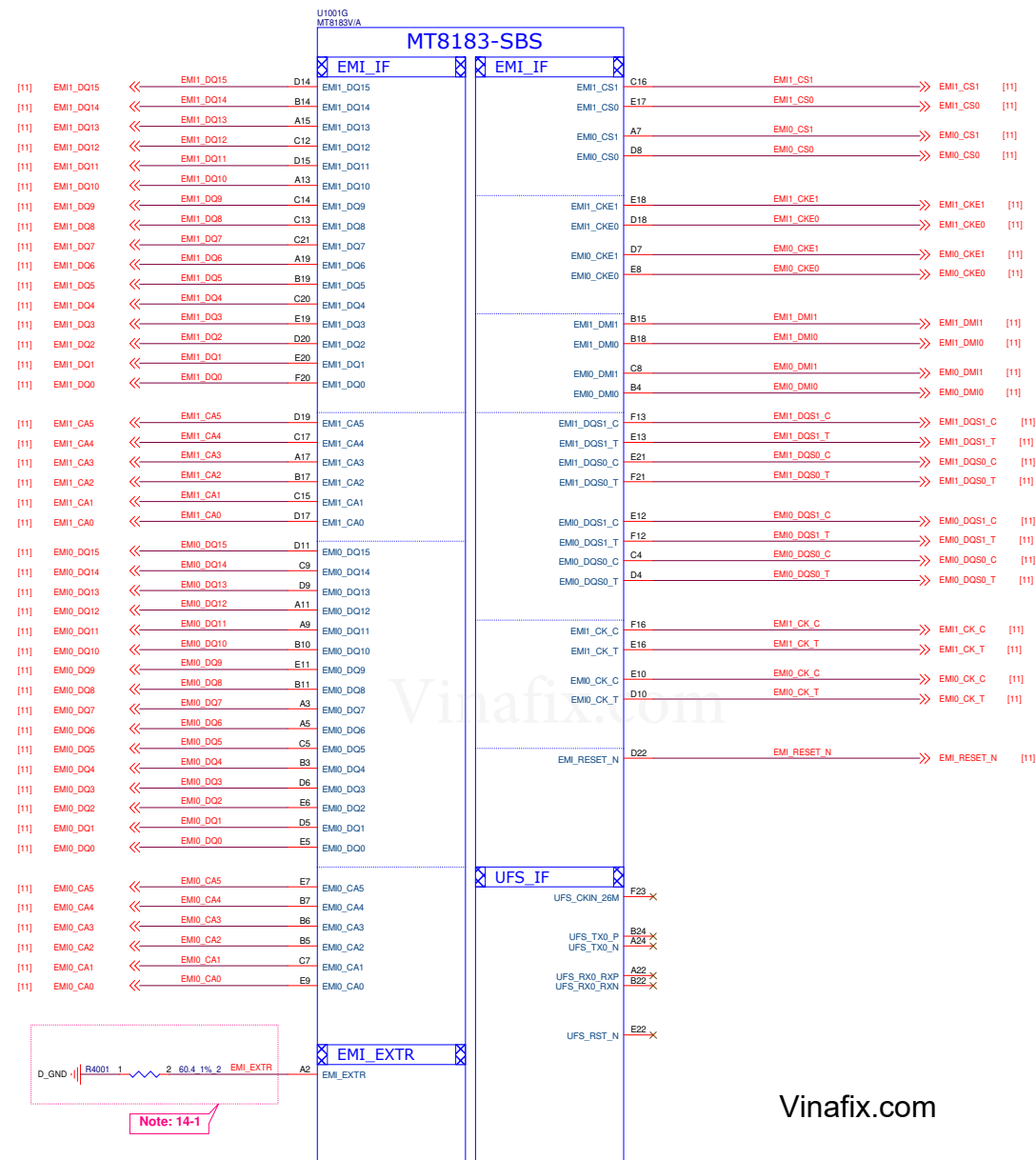
Note 12-3: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-4: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

Note 12-5: AUD_SYNC_MISO and AUD_CLK_MISO are DDR type feature in bootstrap

AUD_SYNC_MISO	AUD_CLK_MISO	DDR
LO	LO	LPDDR4X
LO	HI	LPDDR4X(Ext x 2 EN)
HI	LO	LPDDR3
HI	HI	LPDDR4X(Ext x 1 EN)

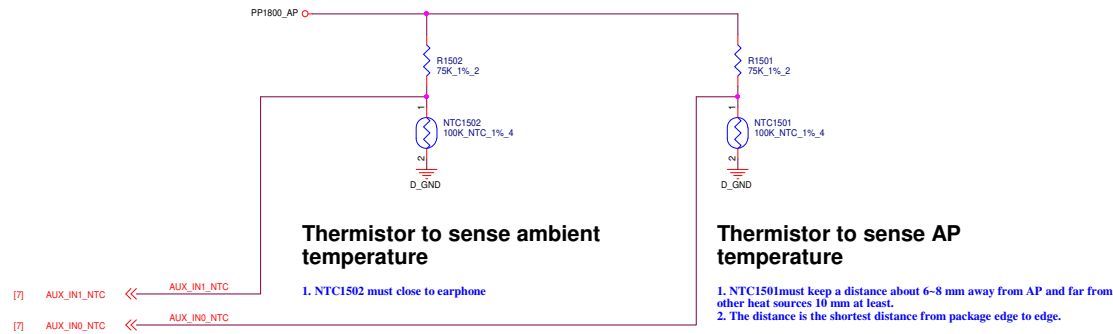




Schematic design notice of "BB_3" page.

Note 14-1: The resistor of EMI_EXTR for DRAM has to be placed near to BB as close as possible
R4001, please select 60.4 ohm 1% resistor

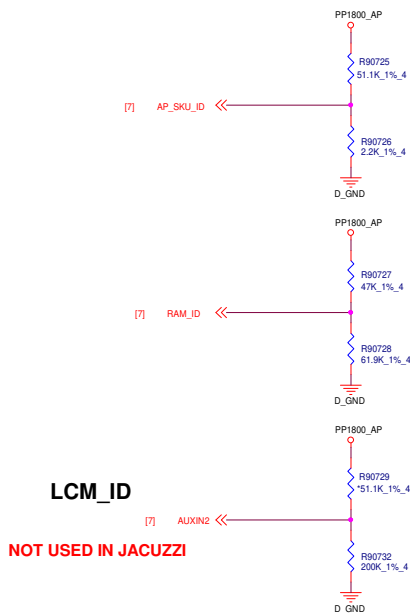
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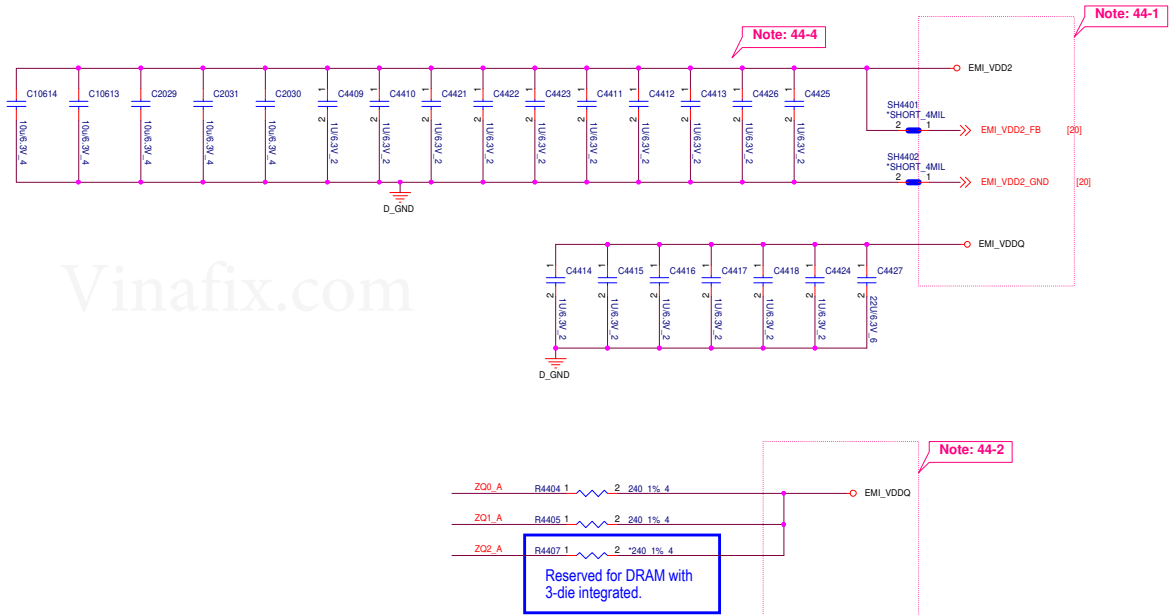
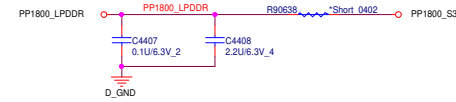
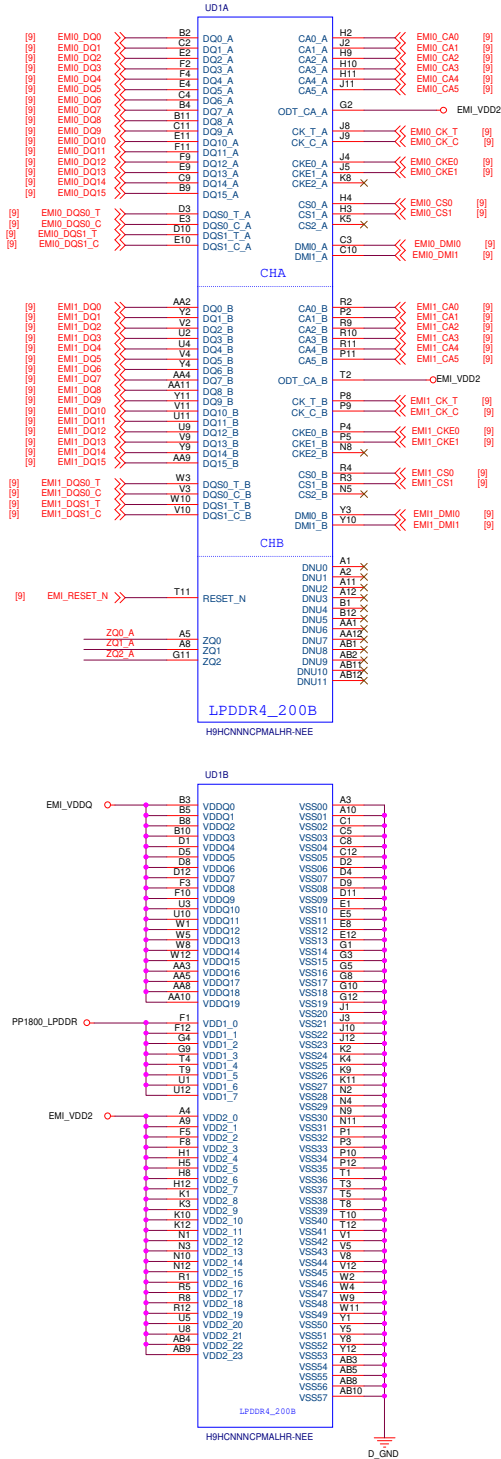
SKU ID (AP AUXIN4)					
NUMERIC ID	RP (KOHM)	RD (KOHM)	VOLTAGE (V)	SKU	VIO (V)
0	51.1	2.2	0.074	0	1.8
1	51.1	6.81	0.212		
2	51.1	11	0.319		
3	57.6	18	0.429		
4	51.1	22	0.542		
5	51.1	30	0.666		
6	51.1	39.2	0.781		
7	56	56	0.900		
8	47	61.9	1.023		
9	47	80.6	1.137		
10	56	124	1.240		
11	51.1	150	1.343		

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RAM ID (AP AUXIN3)						
NUMERIC ID	RP (KOHM)	RD (KOHM)	VOLTAGE (V)	VIO (V)	VENDOR	MPN
0	51.1	2.2	0.074	1.8	SAMSUNG 4GB LP4X	K4UBE3D4AM-MGCJ
1	51.1	6.81	0.212		HYNIX 4GB QDP LP4X	H9HCNNCPMALHR-NEE
2	51.1	11	0.319		MICRON 4GB LP4X	MT53E1G32D4NQ-053 WT:E MT53E1G32D4NQ-046 WT:E
3	57.6	18	0.429		SAMSUNG eMCP: 4GB LP4x + 64GB eMMC v5.1 (MLC)	KMDH6001DA-B422
4	51.1	22	0.542		SAMSUNG eMCP: 4GB LP4x + 64GB eMMC v5.1 (TLC)	KMDP6001DA-B425
5	51.1	30	0.666		MICRON eMCP: 4GB LP4x + 64GB eMMC v5.1	MT29VZZZAD8DQKSL-046 W.9K8
6	51.1	39.2	0.781		SAMSUNG eMCP: 4GB LP4x + 128GB eMMC v5.1 (TLC)	KMDV6001DA-B620
7	56	56	0.900		Sandisk eMCP: 4GB LP4x + 128GB eMMC v5.1	SDADA4CR-128G
8	47	61.9	1.023		SAMSUNG 4GB LP4X	K4UBE3D4AA-MGCL
9	47	80.6	1.137		MICRON 8GB LP4X	MT53E2G32D4NQ-046 WT:A
10	56	124	1.240			
11	51.1	150	1.343			



Ext. EMI_VDD1 for LPDDR4x VDD1

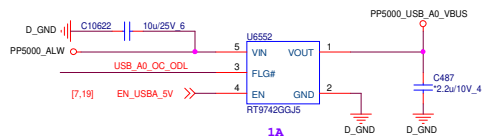
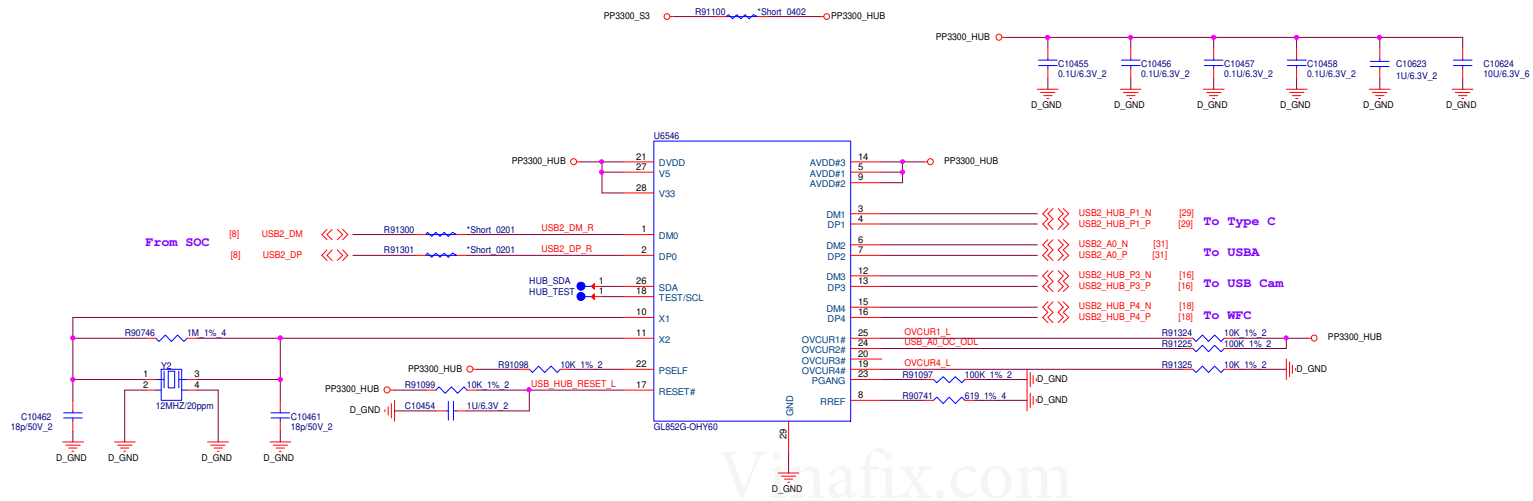


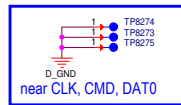
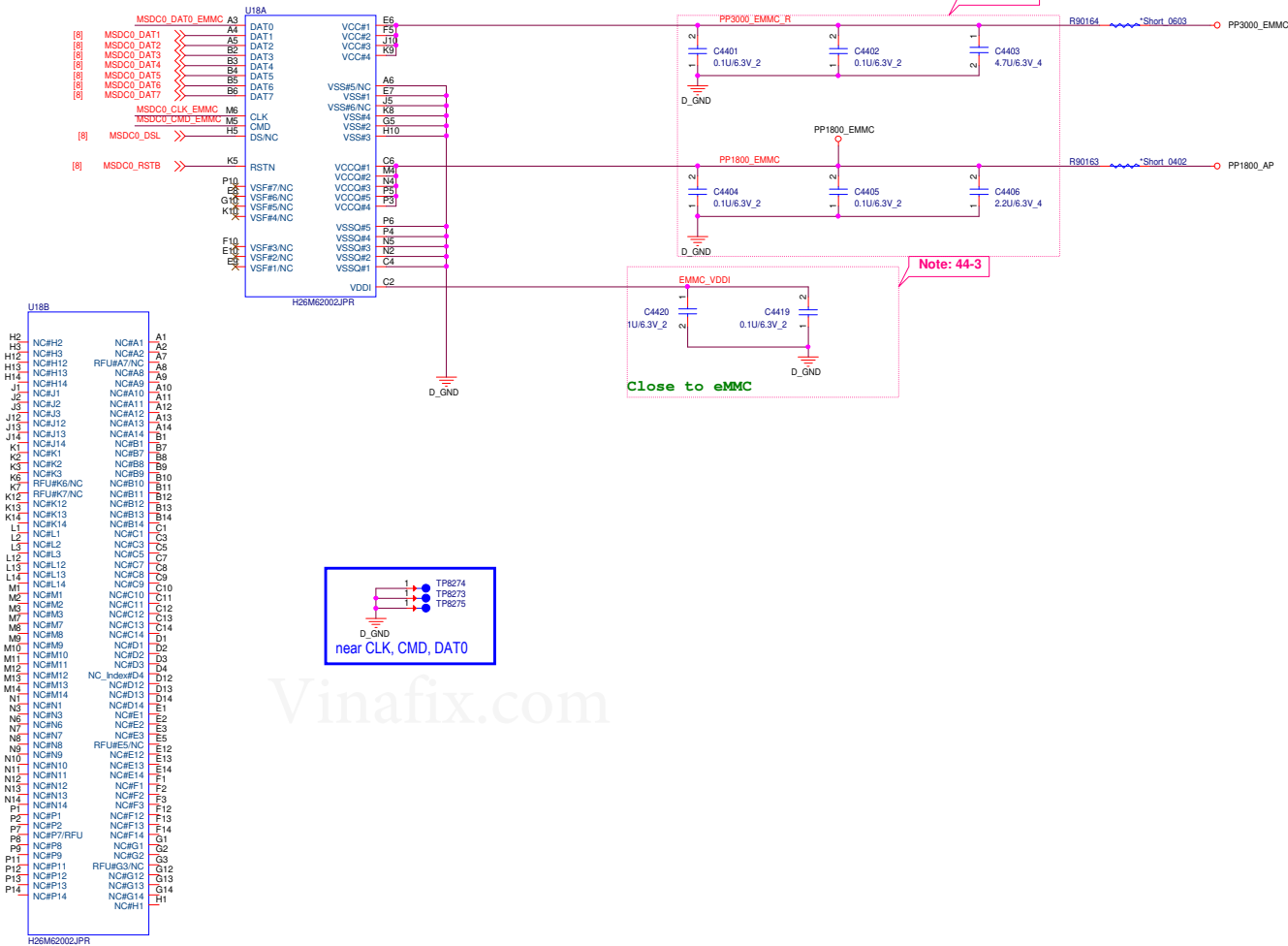
Schematic design notice of "Memory_LPDDR4"

Note 44-1: Please refer to power supply related page select VDRAM 2 / VDRAM1 output voltage properly for LPDDR4

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC (>10uF, at PMIC page):
please also refer to MMD and layout guide for placement.





Layout: trace extension to compensate mux propagation delay ~68ps for DAT1-7 and DS

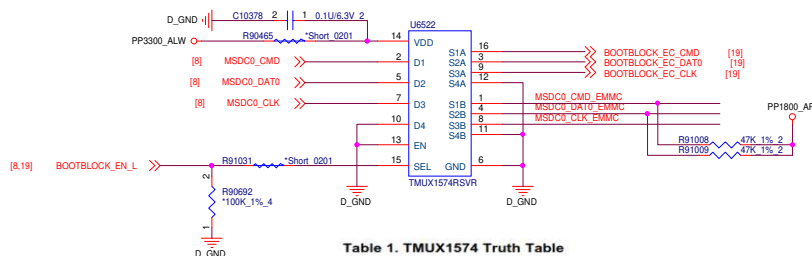


Table 1. TMUX1574 Truth Table

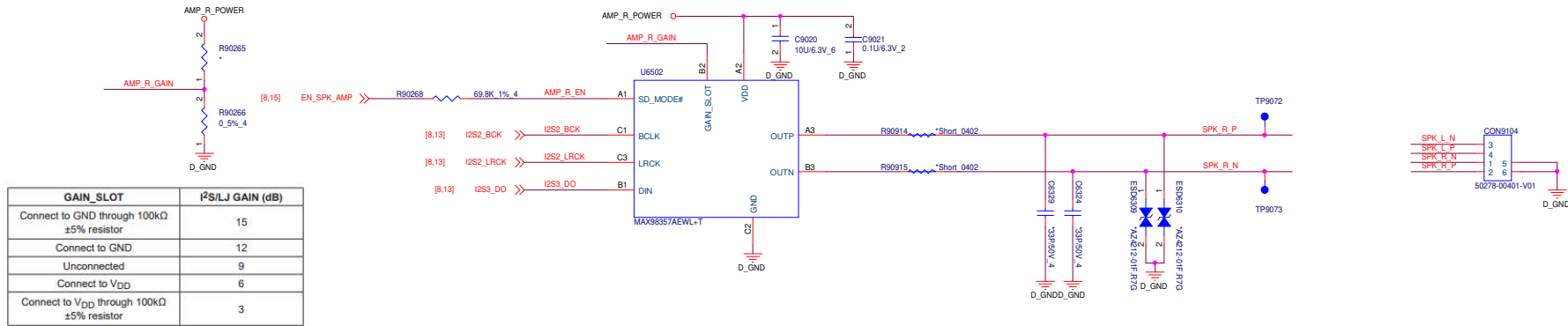
INPUTS		Selected Source Pins Connected To Drain Pins (Dx)
EN	SEL	
0	0	SxA connected to Dx
0	1	SxB connected to Dx
1	X	Hi-Z (OFF)

Schematic design notice of "Memory_eMMC"

Note 44-3: Please refer to vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Speaker Amplifier

5/22 maybe 100K or 0 ohm, depned on gain(DB) now just set to NC



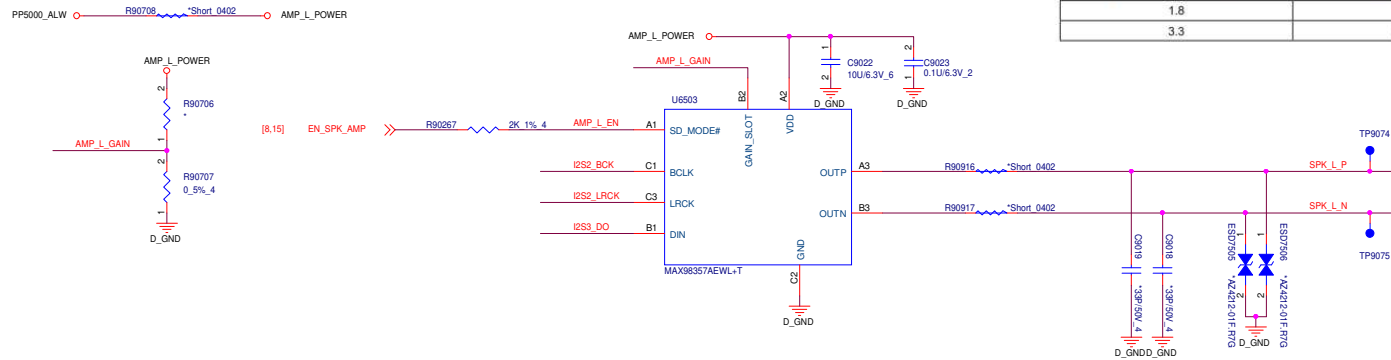
SD_MODE COMPARATOR TRIP POINTS					
		See SD_MODE and shutdown operation for details	0.08	0.16	0.355
B0			0.65	0.77	0.825
B1			1.245	1.4	1.5
B2					
SD_MODE Pulldown Resistor	R _{PD}		92	100	108
					kΩ

Table 5. SD_MODE Control

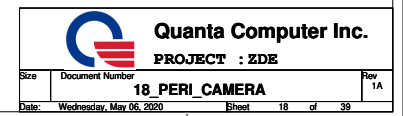
SD_MODE STATUS		SELECTED CHANNEL
High	V _{SD_MODE} > B2 trip point	Left
Pullup through R _{SMALL}	B2 trip point > V _{SD_MODE} > B1 trip point	Right
Pullup through R _{LARGE}	B1 trip point > V _{SD_MODE} > B0 trip point	(Left/2 + right/2)
Low	B0 trip point > V _{SD_MODE}	Shutdown

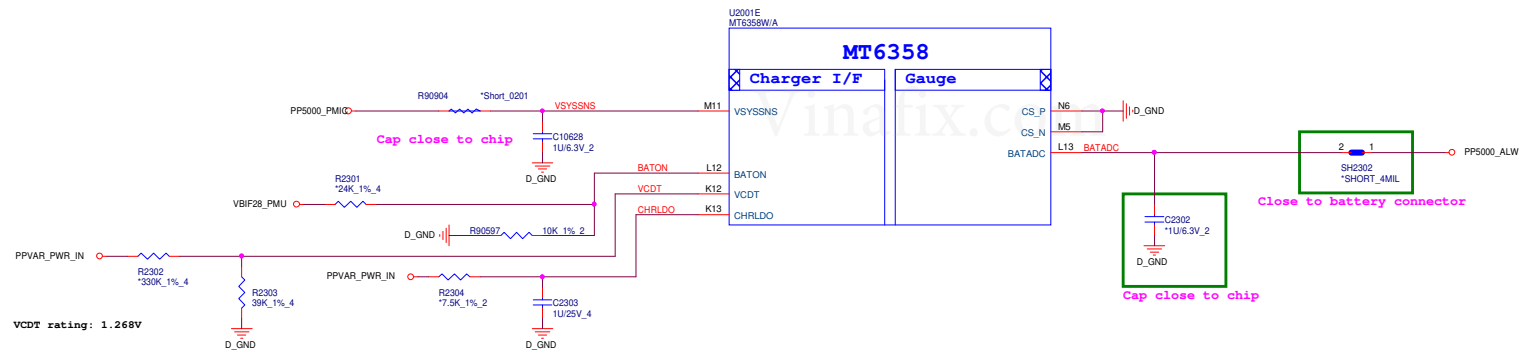
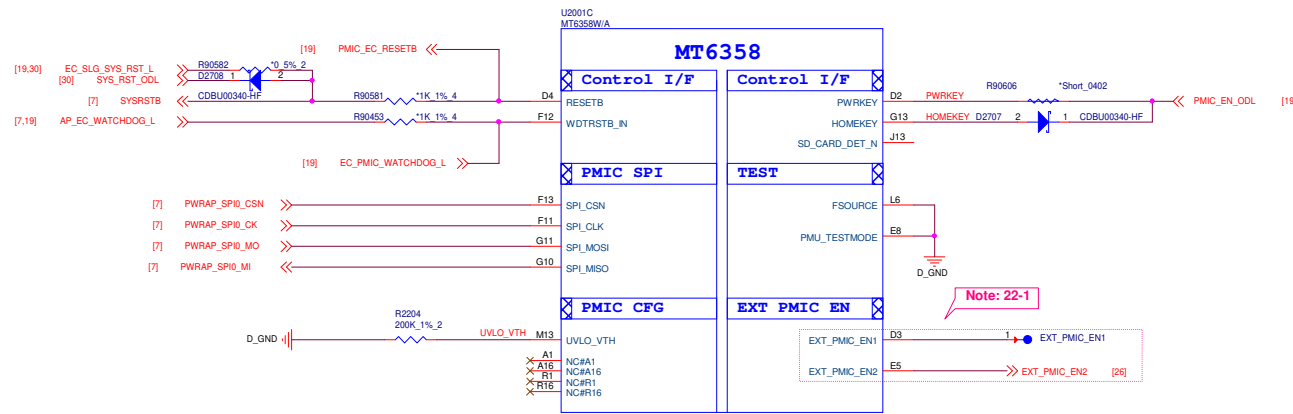
Table 6. Examples of SD_MODE Pullup Resistor Values

LOGIC VOLTAGE LEVEL (V _{DDIO}) (V)	R _{SMALL} (kΩ)	R _{LARGE} (kΩ)
1.8	69.8	300
3.3	210.2	634

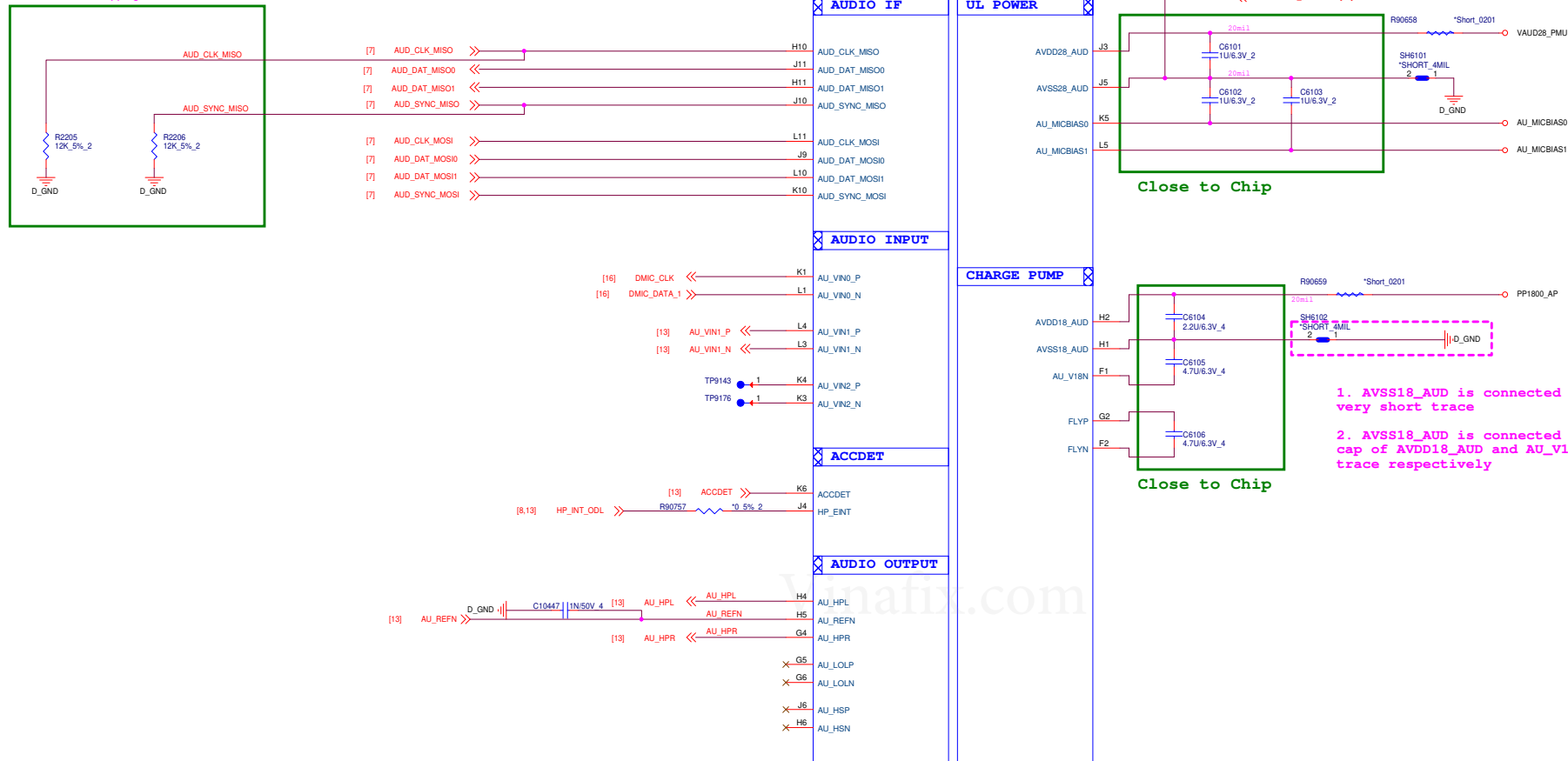



Quanta Computer Inc.
PROJECT : ZDE
 Size Document Number
16 PERI LCD CTP TPAD
 Date: Wednesday, May 06, 2009 Sheet 18 of 30





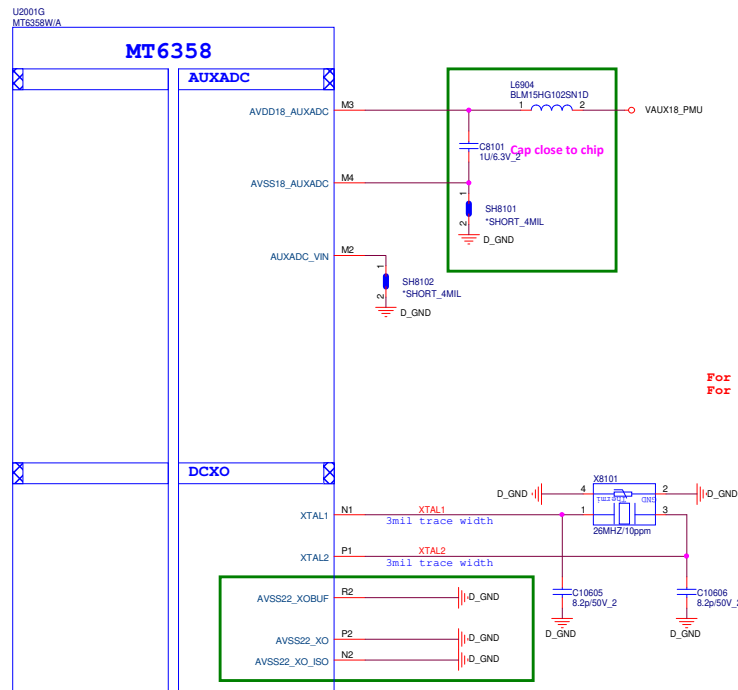
MT6358 HW trapping for DRAM



Schematic design notice of "POWER_MT6358-Audio"

Note 23-1: VDRAM 2 / VDRAM1 output voltage vs. trap pin.

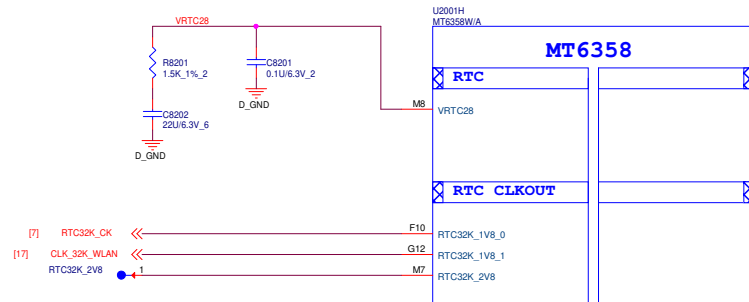
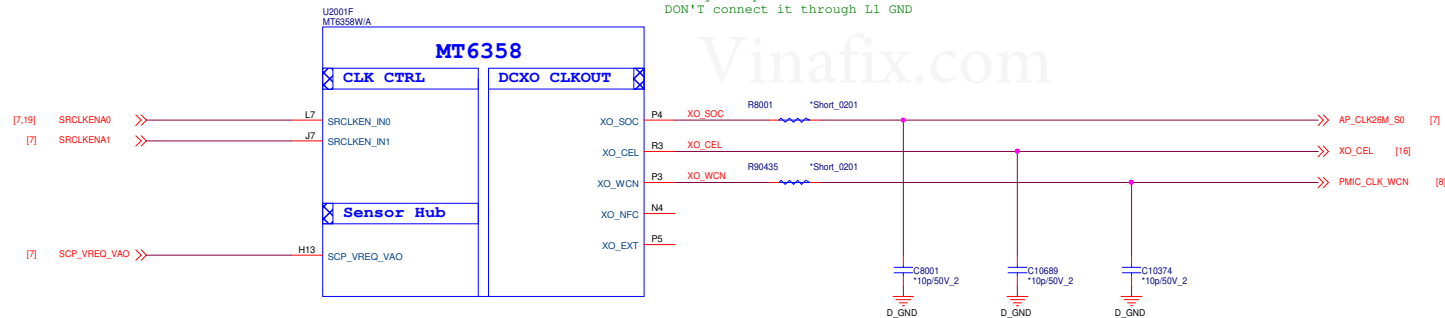
HW GPIO configuration		Trapping Option		DRAM type	VDRAM2 Power source (VS2_LDO1_ball)
AUD_SYNC_MISO	AUD_CLK_MISO	VDRAM1	VDRAM2		
0	0	1.125V	0.6V	LP4X	VDRAM1
0	1	OFF	1.8V	LP4X (Ext x 2 EN)	VS1
1	0	1.225V	OFF	LP3	VDRAM1
1	1	1.125V	1.8V	LP4X (Ext x 1 EN)	VS1

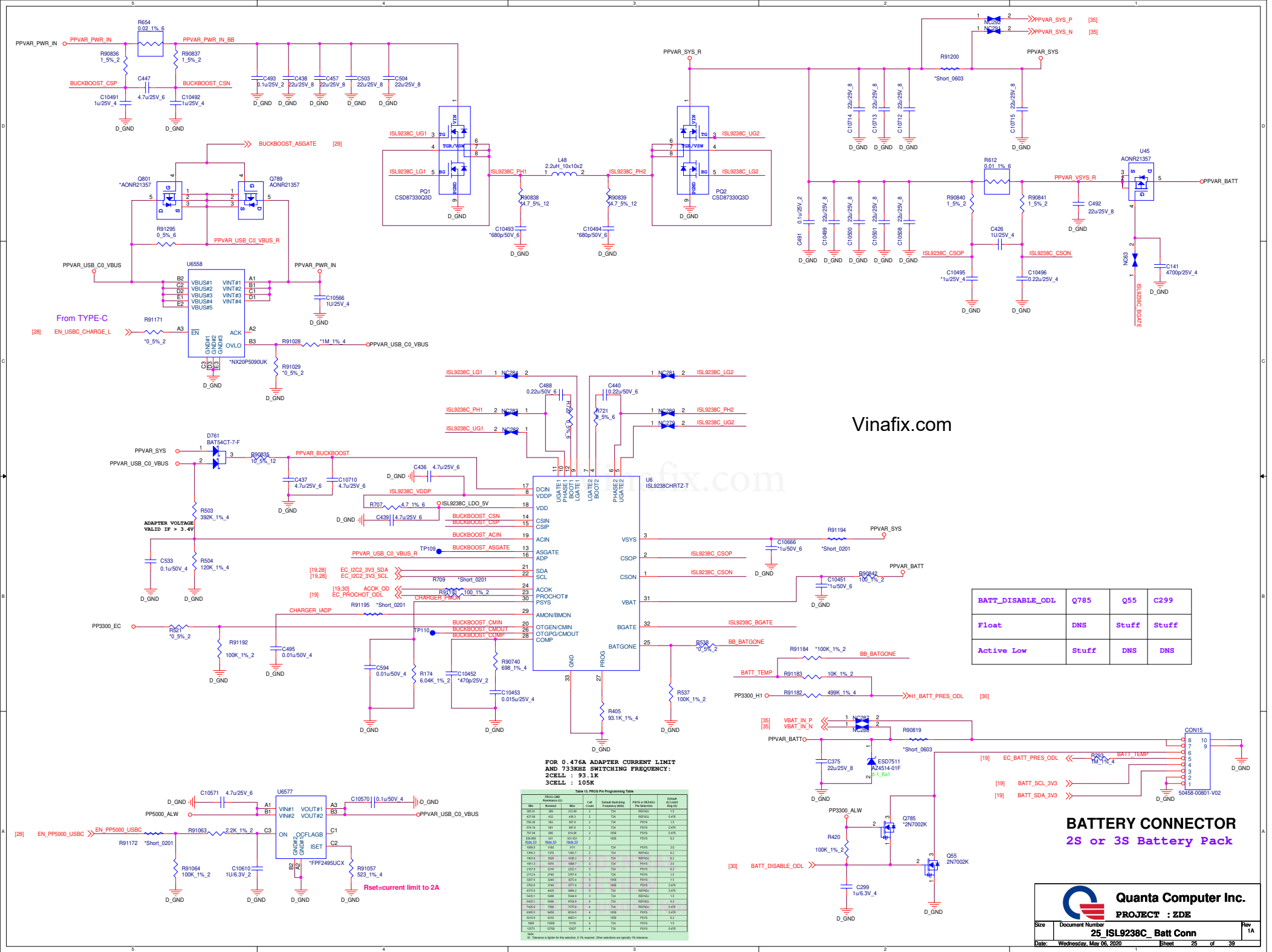


Route AVDD18_AUXADC/AUXADC_VIN with 3mil trace width and with well GND shielding.
AVDD18_AUXADC/AUXADC_VIN need to be shielded with GND or AVSS18_AUXADC.

For MT8183, cap & resistor stuff, R8103, C8102 NC, X8101 using XTAL
For MT8788, cap & resistor DNS, R8103, C8102 stuff. X8101 using TSX

Please connect DCXO GND to main GND by independent L1-2 GND via.
DON'T connect it through L1 GND

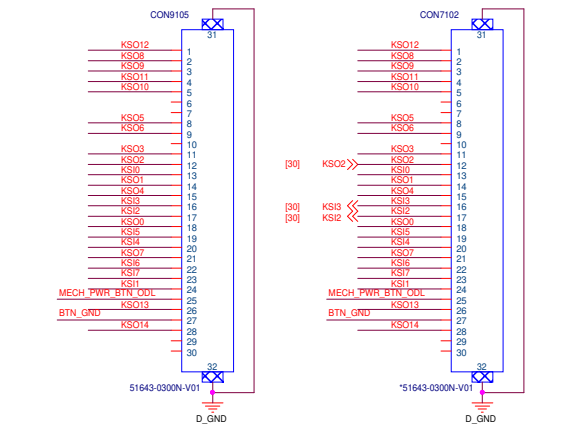




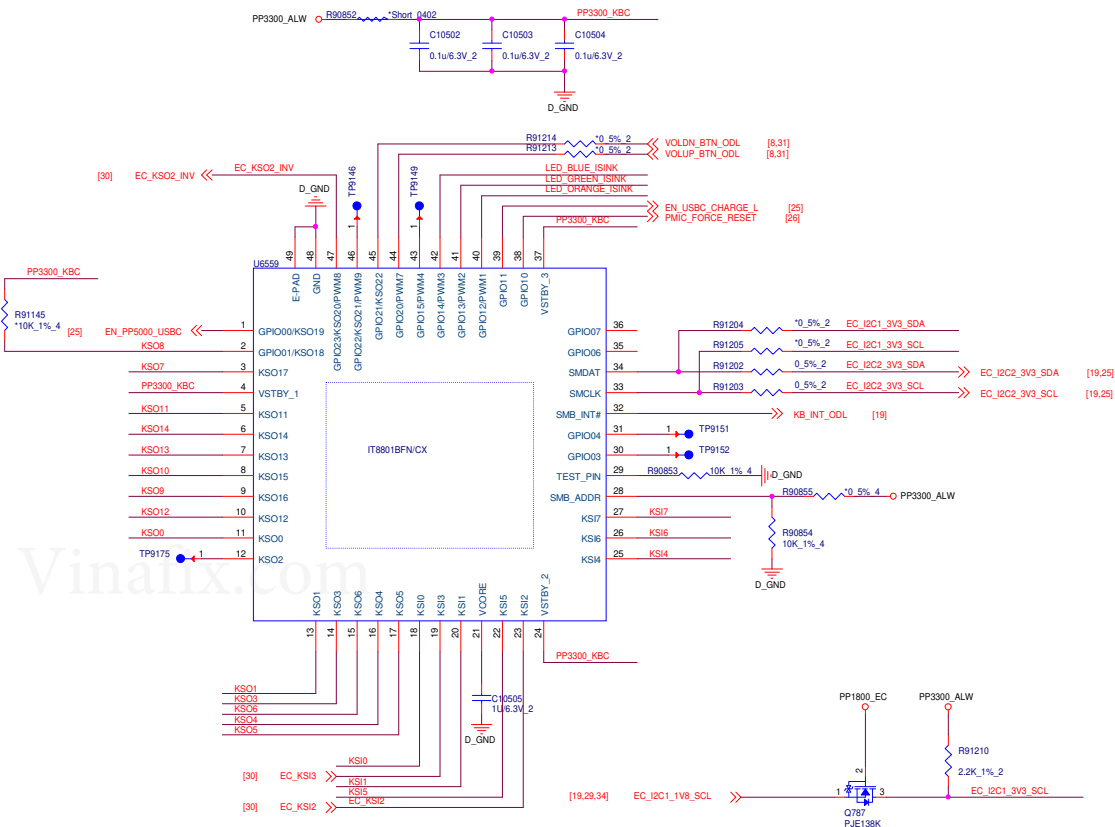
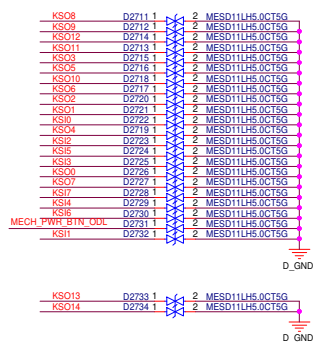
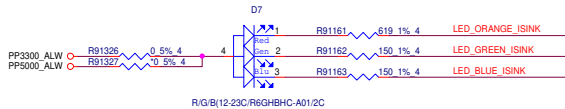
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For 11"

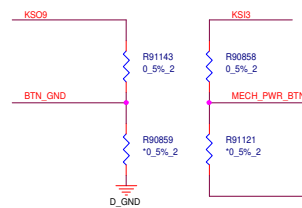
For 15"



CHARGE/BATTERY LED

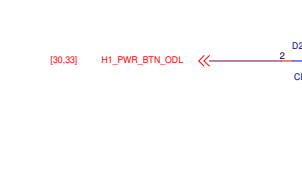


Stuff R91143, R90858 for lock button

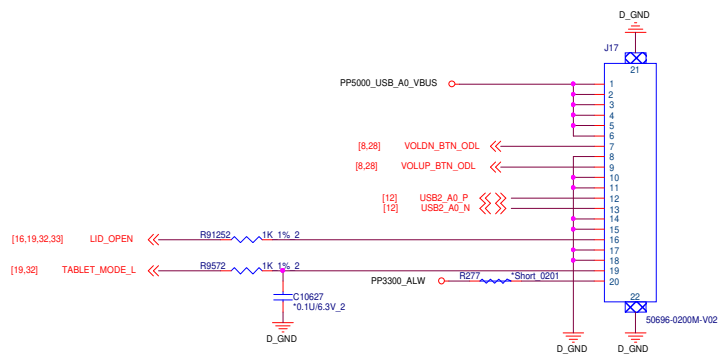


Power Key

Stuff R90859, R91121 for power button



To SUB Board Connector



Force Download key

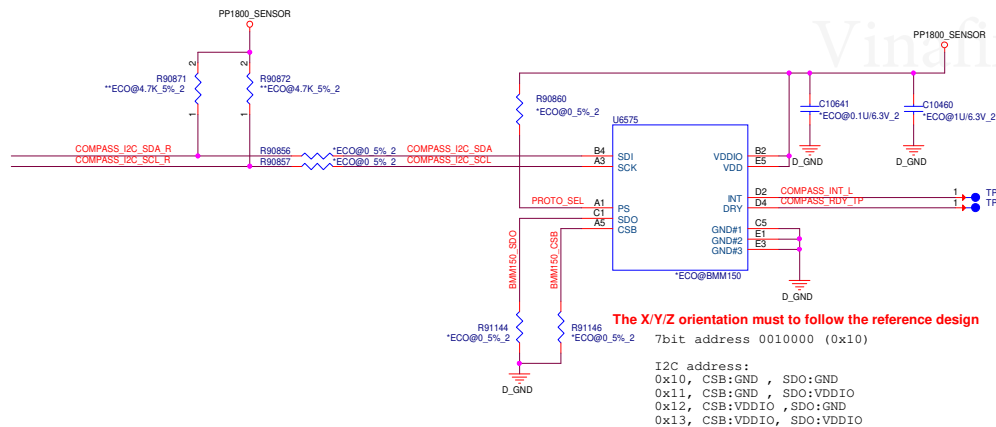
[8,33] MT8183_KPCOL0 << TP9080

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```
I2C address:
0x68, SDO pulled to GND (default)
0x69, SDO pulled to VDDIO
```



COMPASS

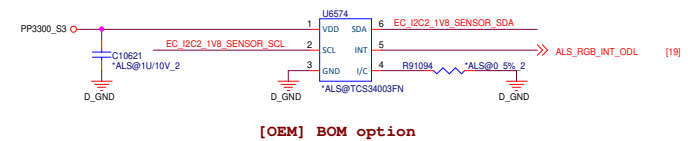


DNS IF GMR IS ON SUB-BOARD



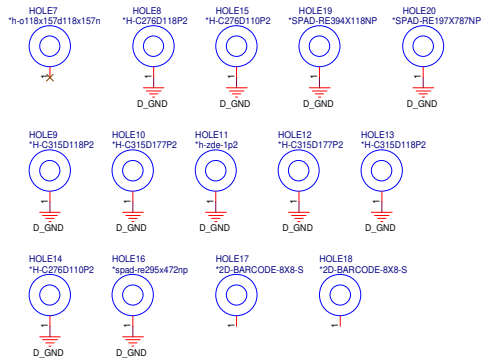
```
I2C MODE: ( SET BY NCS TIE TO VDDIO )
I2C 8bit ADDRESS: 0X3E (SDO_ADDR = VDDIO)
I2C MAX SPEED = 3.4MHZ
```

Ambient Light Sensor

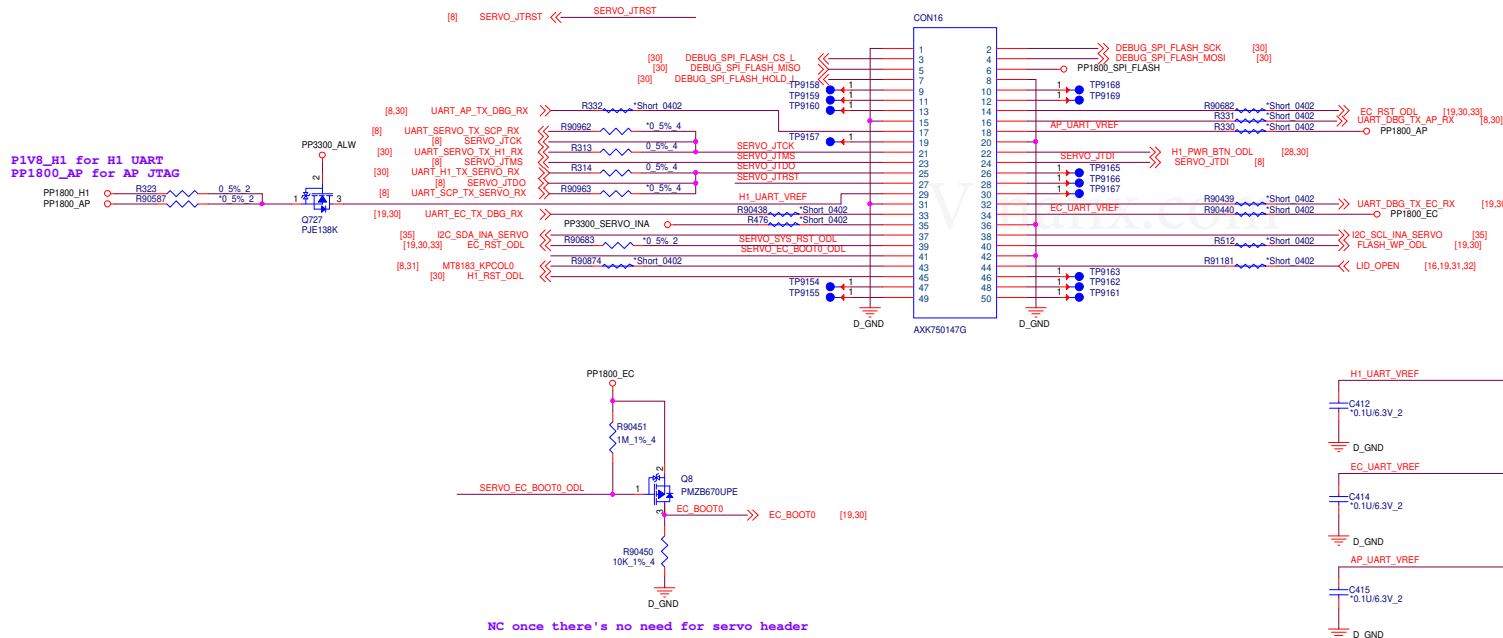
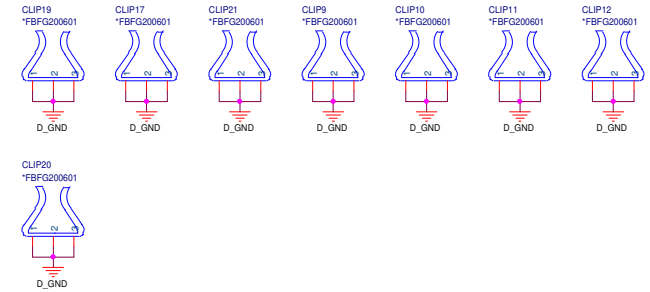


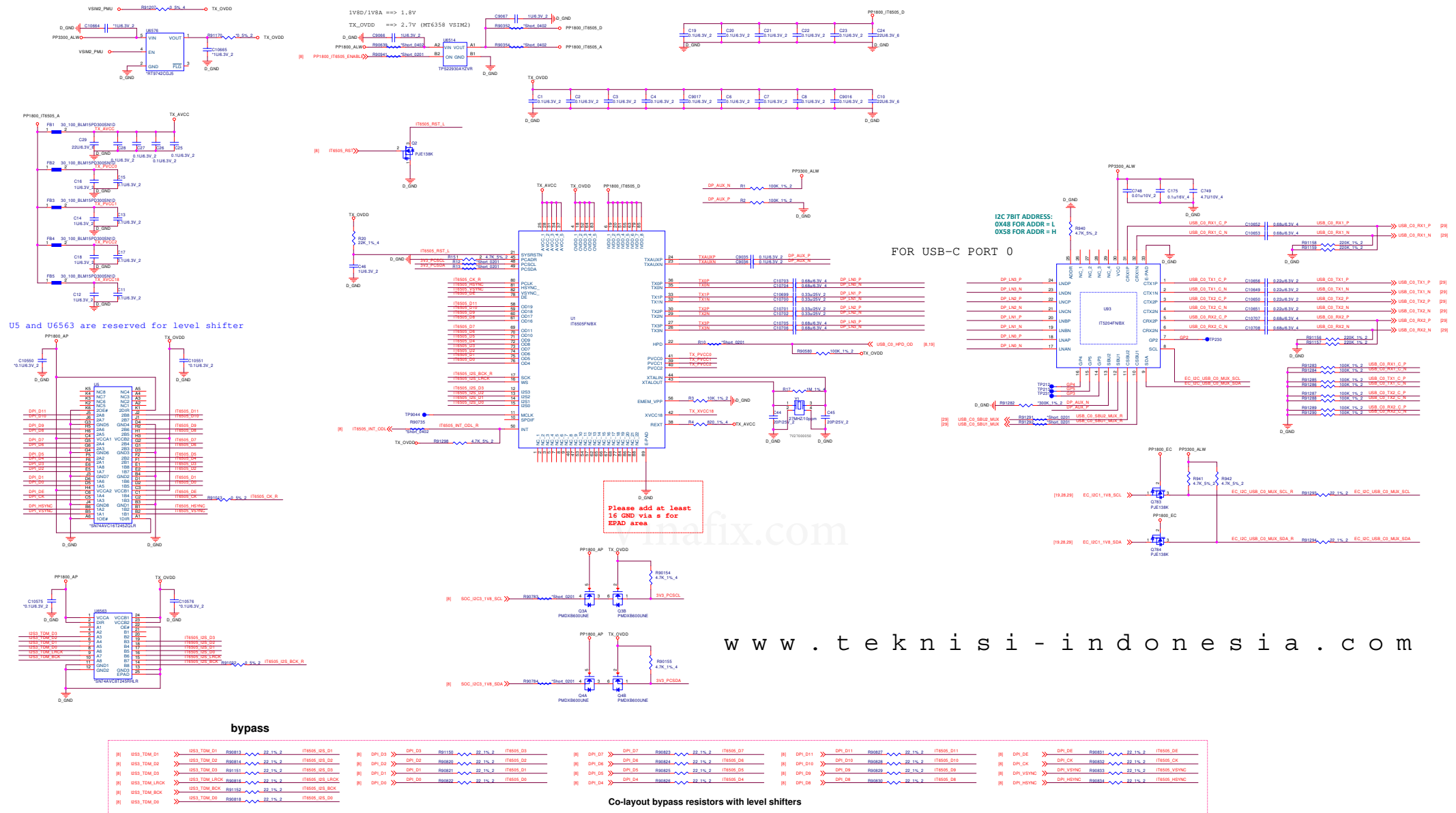
Note 77-7: Interrupt pin of MEMS sensor must be assign to ball EINT[12:0]

HOLE

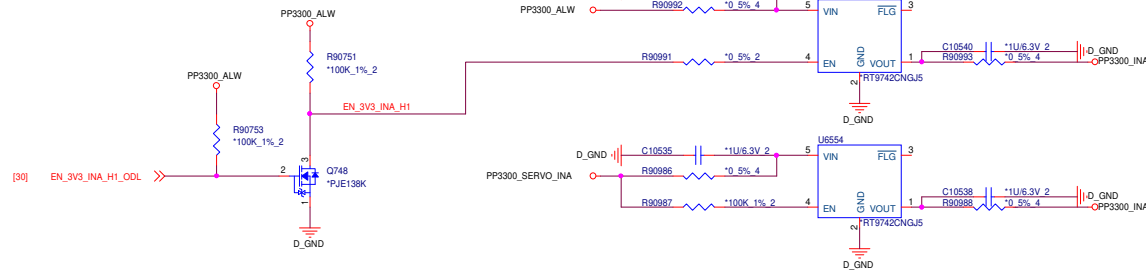
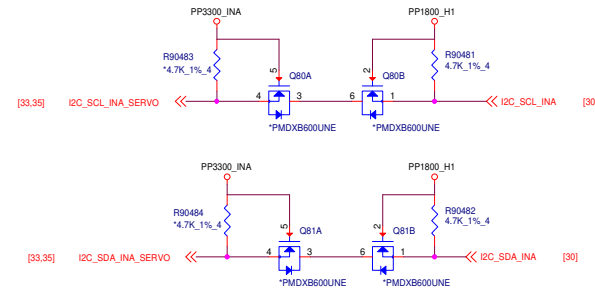
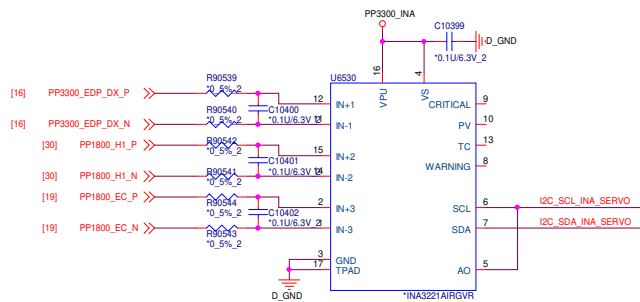
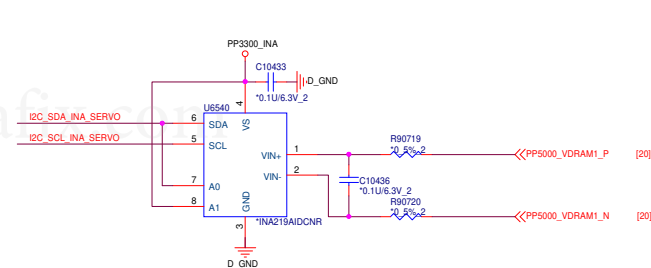
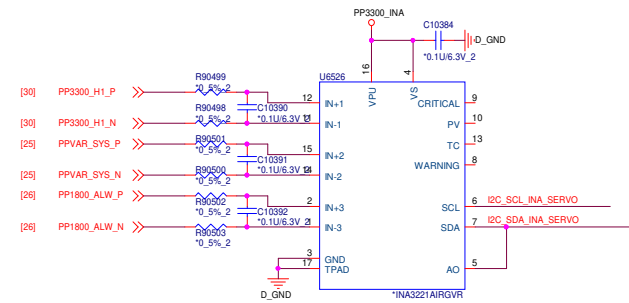
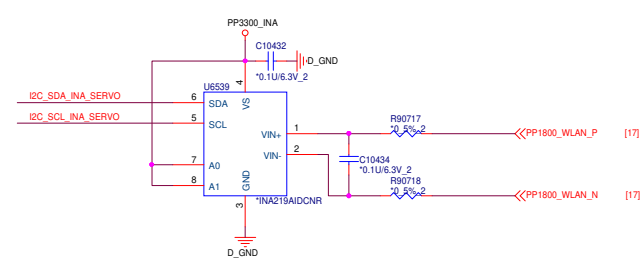
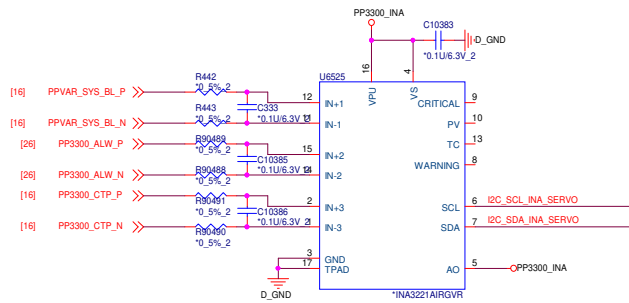
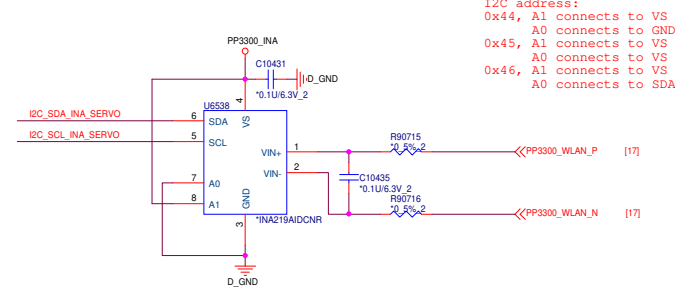
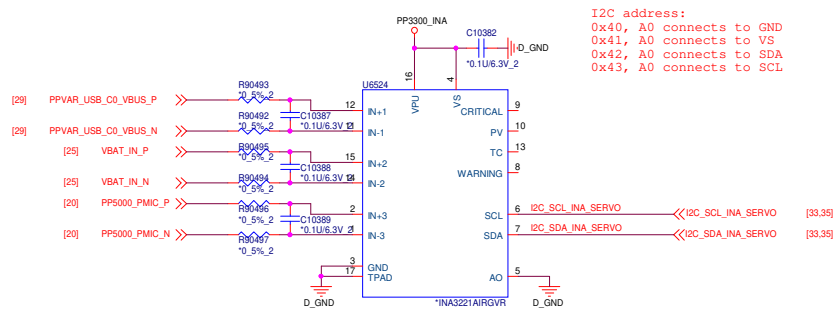


Clip





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Data	Page	Item
5/27	16	change CON6801 & J19 to Bobba360 eDP panel connector J15(include DMIC connection too)
5/27	25	remove R90739, ISL9241_BYPSG, ISL9241_NGATE test point, add circuit as note pic
5/27	25,30	Add inveter circuit for BATT_DISABLE_ODL net (PU 100K to PP3300_ALW) that connects to Battery Conn.
5/27	25	Add a power symbol ISL9241_5V for ISL9241 VDD (pin18)
5/28	30	U124 B4 pin connects to KSI2, A5 pin connect to EC_KSO2_INV, A8 pin connects to EC_KSI2, B8 pin connects to KSO2
6/3	7	AE24 pin net name PANEL_3V3_ENABLE, AE25 net name LCD_POWER_EN connect to page 16, AJ25 pin net name USB_POWER_EN connects to page 12
6/3	16	change R91125 connects to PP3300_S3
6/3	16	remove U6549 circuit
6/3	16	change R90695 connect to PP3300_S3
6/3	12	change U6552 to 0.5A PN
6/3	16	VSYS_BL_P/VSYS_BL_N connect to R391. Maybe move R391 to VSYS/R259 location is more better
6/3	19,32	change GAUGE_INT_ODL to RGB_INT_ODL connects to page U6574 pin 5 . R90865 remove
6/3	34	add DPI/I2S level shift circuit & 3.3V power back as backup for PCB size
6/4	1	Update block diagram
6/4	17	consider to remove U6534, U6535 circuit.
6/10	16	Please change U260 from LDO(RT9018) back buck converter(RT5710)
6/10	25	Please connect replace PPVAR_PWR_IN with PPVAR_USB_C0_VBUS.
6/11	25	AONP36336 and AONR36336 seem to have better power efficiency than SISA14DN. Please double confirm if there are other concerns like cost and thermal to replace SISA14DN with AONP36336x2 or AONR36336 x 4.
6/11	29	Change U6533 pin A2 from VBUS to PPVAR_USB_C0_VBUS
6/14	28	- add 0 ohm between LED_1_L and GPIO12/PWM1 of IT8801.- add 0 ohm between LED_2_L and GPIO13/PWM2 of IT8801. - add one more power led and LED_3_L to GPIO14/PWM3 of IT8801. (b/135086465)
6/14	25	A bi-directional power switch is required between USB-C connector and charger input: please add AOZ1375DI
6/14	28	RGB_INT_ODL to U6559.38 (IT8801), and add TP to all unused pins of IT8801
6/14	30	Add 0 ohm between EC_KSO2_INV and H1
6/14	34	Add USB-C MUX (IT5205) in order to resolve USB3.0 detection issue
6/18	25	Reserve a 0 ohm to bypass U6562
6/18	26	Change U6569 to RT6214HRGJ8F, PG is needed for PP1800_ALW_PG
6/18	1	Update the block diagram
6/18	12	Add WFC using DM4 and DP4 of U6546
6/18	16	Replace LCD_POWER_EN circuit with a fuse, and add another 1uF on EDP_BL_VOUT
6/18	28	DNS R90875 since there's internal pull up, and change net name from KB_VSTBY to PP3300_KBC
6/18	28	Assign LID_ACCEL_INT_L to U6559.39 (GPIO11)
6/18	34	For I/O power of IT6505 (TX_OVDD), please add a power switch and use VSIM2_PMU as enable pin. PS. For proto build, please pick 3V3 as default route
6/18	34	(a) AC caps on SSTX lines should be 0.1uF; while AC caps on SSRX lines are 0.33uF (b) From loss perspective, please use 0201 size for caps and resistors on SSTX/SSRX lines (and void pads in layout)
6/18	34	[Netname fix] DDIO_TX*_P -> DP_LN*_P; DDIO_TX*_N -> DP_LN*_N; DDIO_AUX_P -> DP_AUX_P; DDIO_AUX_N -> DP_AUX_N; AUX+ -> USB_C0_SBU1_MUX; AUX- -> USB_C0_SBU2_MUX
6/18	29	FSUSB42UMX is not required, please follow h1 ref.
6/18	34	Connect IT5205 to EC_I2C1_1V8_* with level shifts, and mount R941/R942
6/18	25	Remove AOZ1375DI since it does not support dead battery mode. Please follow kukui using U6561(FPF2495UCX) and U6558 (NX20P5090UK), EN_USBC_CHARGE_L and EN_PP5000_USBC.
6/18	19	Update EC GPIO pin assign
6/20	30	DNS/NC R90640
6/20	30	Add netname onto U124.J5: EC_BOOT_DFU
6/20	33	Please reserve testpoints onto servo header NC pins
6/20	33	[Netname for nit] DEBUG_UART_POWER -> AP_UART_VREF ; DEBUG_EC_UART_POWER -> EC_UART_VREF ; H1_DEBUG_POWER -> H1_UART_VREF ; LID_OPEN_L -> LID_OPEN
6/20	33	Connect LID_OPEN to servo header pin44 via a 0ohm
6/20	28	Remove EC_WAKE and the interrupt OR circuit
6/20	19	KB_INT_ODL to EC's PA8 with a 0 ohm
6/20	30	Remove PWRBTN, PWRBTN_R and add TP on U6548.4
6/20	28	The note in p28 about R90857, should be R91143
6/20	30	Reserve 0 ohm bypassing U12A.3->1 and U12B.5->7
6/20	32	Add a mosfet onto LID_ACCEL_INT_L as level shift
6/20	12	Reserve a 0-ohm resistor array (can be replaced by EMI choke) for DP/DM near USB-A connector
6/20	12	[For nit] 2. USB_A_POWER -> PP5000_USB_A0_VBUS 3. USB_HUB2_DM -> USB2_A0_N 4. USB_HUB2_DP -> USB2_A0_P 5. TYPEC0_USB_DM -> USB_C0_USB2_N 6. TYPEC0_USB_DP -> USB_C0_USB2_P 7. USB_HUB1_DM -> USB2_HUB_P1_N 8. USB_HUB1_DP -> USB2_HUB_P1_P 9. USB_HUB3_DM -> USB2_HUB_P3_N 10. USB_HUB3_DP -> USB2_HUB_P3_P 11. HUB_USB4_DM -> USB2_HUB_P4_N 12. HUB_USB4_DP -> USB2_HUB_P4_P 13. USB_WFC_N -> USB2_WFC_N 14. USB_WFC_P -> USB2_WFC_P 15. VSYS_PMIC -> PP5000_PMIC 16. VSYS_PMIC_P -> PP5000_PMIC_P 17. VSYS_PMIC_N -> PP5000_PMIC_N 18. PMIC_FORCE_RESET_OD -> EN_PP5000_ALW_L
6/20	1	Update block diagram
6/20	19	Change netname from OTG_EN to EN_OTG
6/20	29,30	Remove R90585/Q719/R90586, re-connect AC_PRESENT to ACOK_OD and add a 100kOhm pull-up to PP3300_H1
6/20	19	EN_USBC_CHARGE_L to EC's PC7, EN_PP5000_USBC to PD2
6/20	25	Remove J927 and related components, change H1_CHASSIS_OPEN to H1_BATT_PRES_ODL with 499K pull up to PP3300_H1
6/20	26	Add a test point on PP3300_ALW_PG
6/20	25	Remove R58 and CD5, add 100k serie resistor from EC_BATT_PRES_ODL to R293
6/20	25	Battery I2C interface should be connected to EC_I2C2_3V3
6/20	25	Change ISL9241 I2C interface to EC_I2C2_3V3
6/20	25	PPVAR_CHG_VIN should be replaced by PPVAR_PWR_IN.

Data	Page	Item
6/20	25	1. Add netname to CON15.5 "BATT_TEMP" 2. Change R293 to 100kOhm 3. Connect BATT_TEMP to H1_BATT_PRES_ODL via a 0ohm 4. Connect BATT_TEMP to BB_BATGONE via a DNS'd 100kohm
6/20	25	Change BATT_TEMP circuit
6/21	32	Remove note "IMU sensor has to be placed as close (<4cm) to WF CAM"
6/21	19,32	ACCEL_INT_ODL -> BASE_ACCEL_INT_ODL
6/21	25	Change charger IC to ISL9238
6/21	34	Change C10649,C10650,C10651,C10656 to 0.22uF
6/21	19	Reserve an external pull resistor on EC PA14. (1k ohm to PP1800_EC)
6/21	19	- Reserve an external pull resistor on EC PC13. (100k ohm to PP1800_EC) - R91178 can be DNS
6/21	16	Change the backlight control
6/24	14	Remove R90723
6/24	19	Add testpoints on EC's unused pins
6/24	28	Reserve stuffing options for IT8801 on EC_I2C1
6/24	10	DNS R90729 since LCM_ID will not be used for Jacuzzi
6/24	12	Add a note near CON481 "Change to USB2 connector from EVT"
6/24	12	Add capacitor(s) on PP5000_USB_A0_VBUS near USB-A connector, the total capacitance should be >120uF by spec.
6/24	16,19,25,26	[Netname] 1. EN_PP5000_ALW_L -> PMIC_FORCE_RESET 2. VSYS -> PPVAR_SYS
6/24	12,19	1. Change USB_A_POWER_EN to EN_USB_A_5V 2. Connect EN_USB_A_5V to EC's PC14 3. Reserve connection to USB_A_POWER_EN via a DNS's 0Ohm
6/24	-	[Netname] 1. ISL9241_5V to ISL9241_LDO_5V 2. RGB_INT_ODL to ALS_RGB_INT_ODL 3. LID_ACCEL_INT_L to LID_ACCEL_INT_ODL
6/24	30	Change R91116 / R91115 from Q762.3/Q763.3 to Q762.2/Q763.2
6/24	30	Change Q762.1/Q763.1 from PP3300_H1 to ISL9241_LDO_5V
6/24	28	1. LID_ACCEL_INT_ODL to EC's PA14, no external pull high 2. ALS_RGB_INT_ODL to EC's PC4, no external pull high 3. Reserve TP on IT8801 side
6/24	34	Having a 0 ohm from VSIM2_PMU to TX_OVDD, DNS U6576
6/24	22	PPVAR_CHG_VIN is signal net, should change to PPVAR_PWR_IN
6/24	25	Check battery spec to determine stuffing option of Q785/Q55/R420/C299.
6/24	25	Adding 20m ohm between PQ2.1 and VSYS, connect to VSYS_P / VSYS_N instead of R612
6/24	25	Reserve ASGATE control with PFET from PPVAR_USB_C0_VBUS to PPVAR_PWR_IN
6/24	10,19	Please complete HWID tables in schematic
6/24	16	1. Rename TP_INT_1V8 to TRACKPAD_INT_1V8_ODL, with an external 100kOhm pull-up 2. Remove Q733 and R91114 3. Change Q732 & Q734 design similar as in column K 4. Please use 100kOhm for external pull-up on interrupt
6/25	19,32	1. Use SPI as default interface from EC to BMI160, and reserve I2C 2. EC pins need to be moved around, please see link in column K
6/25	8	1. Connect EC_VOLUP_BTN_ODL to AP's EINT5 via a 0ohm 2. Connect EC_VOLDN_BTN_ODL to AP's EINT6 via a 0ohm
6/25	25,30	[Netname] *9241 to *9238C
6/25	30	[BOM] 1. DNS U12, R91088, R90386, R90387, R91188, R91189, C10620 2. STUFF R91115, R91116
6/26	19	[BOM] Stuff U6547/ Q750 / R90880 / C10469
6/27	19	[BOM change] For Jacuzzi, we decided to reset EC_BOARD_ID. Please change R90473 to 2.2kOhm and modify the table accordingly
6/27	30	Kukui post_p2 #28 didn't get introduced: 1. Update reset map to v2.3 2. Change R90973 & R90410 to 4.7kOhm (and modify the strap table)
6/27	8	Note near R90591: "Remove JTAG connections after proto"
6/27	10	Note near LCM_ID: "NOT USED IN JACUZZI"
6/27	25	[BOM change] 1. Mount Q789 2. DNS U6558 and U6577
7/19	25	ISL9238C ds suggests C437 to be at 50V rating, to have effective capacitance higher than 0.4uF at 20V
7/19	30	DNS R91087, R91089, R91092, and R91093
7/19	1,2	Please update block diagram and I2C table accordingly
7/19	16	DNS R218 as RT5710AHGQW cannot stand PPVAR_SYS as input power
7/19		LCM_RST_L_1V8 -> MIPIBRDG_PWRDN_L_1V8 ; EC_VOLUP_BTN_ODL -> VOLUP_BTN_ODL ; EC_VOLDN_BTN_ODL -> VOLDN_BTN_ODL ; PS8640_1V2 -> PP1200_MIPIBRDG PS8640_VIN -> PP3300_MIPIBRDG_DX ; PP3300_LCM -> PP3300_EDP_DX ; PP3300_PANEL -> PP3300_EDP_DX_R ; PP3300_LCM_P -> PP3300_EDP_DX_P PP3300_LCM_N -> PP3300_EDP_DX_N ; PANEL_3V3_ENABLE -> EN_PP3300_EDP_DX
7/19	12	Connect U6552 FLG pin to U6546 OVCUR2# pin, with a 100kOhm external pull-up and netname USB_A0_OC_ODL
7/19	29	Fix typo: Brealdown to Breakdown
7/19	4	Add power tree into schematics
7/25	19	Remove the following connections to EC: - CHARGER_PMON (R91177) - EN_OTG (R91193/R91180) - CHARGER_IADP (R91176)
7/25	29	Need to have discharge path on PPVAR_USB_C0_VBUS. Adding a NFET which is controlled by U6517.PB6 with 1.2K (0603) discharging resistor. The net name is USB_C0_DISCHARGE.
7/25	25	[Net name] 1. VBAT to PPVAR_BATT 2. VSYS_BL_* to PPVAR_SYS_BL_* 3. VSYS_P to PPVAR_SYS_P, VSYS_N to PPVAR_SYS_N 4. VSYS_SMPS to PP5000_SMPS 5. VSYS_V* to PP5000_V*
7/25	19	Remove note "reserved to enable PP1800_EMMC for developing only"
7/25	2	Please update the i2c table for jacuzzi and add ec i2c block diagram
7/25	25	Swap polarity of VBAT_IN_N/VBAT_IN_P on R90819
7/25	19	DNS R91208, since driver is not using LID_ACCEL_INT_ODL
7/25	26	Change R90668 to 0603 package
7/30	7,16	VDDIO_MIPIBRDG_EN -> EN_PP3300_MIPIBRDG_DX
7/30	34	Change USB-C MUX from IT5205 to IT5204 for cost benefit
7/30	19	Change R90880 to 100kOhm to save power when write protection is off
8/8	28	Reconnect EC_KSO2_INV to IT8801 pin KSO20 via a 0ohm
8/8	13	Add note for DA7219: THE TWO SENSE SIGNALS NEED TO BE CLOSE TO THE JACK CONNECTOR ROUTE HP_RING2 AND HP_RING2_SENSE TOGETHER (TREAT AS DIFF PAIR EXCEPT NO NEED FOR IMPEDANCE CONTROL) THE SAME APPLIES TO HP_SLEEVE AND HP_SLEEVE_SENSE SIGNALS ROUTE HP_RING2, HP_RING2_SENSE, HP_SLEEVE, HP_SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE

Data	Page	Item
8/13	4	Update power tree
8/13	28	[OEM] Add keyboard backlight circuit
8/13	28	[OEM] Reserve CON9105 Keyboard connector for 15"
8/13	31	[OEM] Change to sub board connector to 20pin
8/13	12,31	[OEM] Move USB connector to sub board
8/13	16	[OEM] Remove 2nd DMIC
8/13	7,16	[OEM] Change PS8640QFN56GTR2-A0 to ANX7625BN-AC-R ; Rename PP1200_MIPIBRDG_EN to PP1000_MIPIBRDG_EN ; R219 change to 147Kohm ; Add U6579 for ANX7625 1.8V
8/15	33	Change R91181 from 0 ohm to 1k ohm.
8/15	29	[OEM] Change ESD protect for cost benefit : Change U2,U3 from RCLAMP0524PATCT to AZ1045-04F.R7G ; Change D1 from RCLAMP0502BATCT to AZ4024-01F.R7GR Change ESD7105,ESD7106 from ESD73031N-2/TR to PESD5V0X2UM ; Change ESD7102 from AZ4520-01F.R7G to PE3620M1Q
8/15	32	[OEM] Reserve GMR circuit
8/20	19	Connect EC_PROCHOT_ODL to EC pin PC13, not PC14
8/20	2	Update block diagram and I2C table accordingly
8/20	29	Add a 1MOhm pull-down on USB_C0_DISCHARGE, to avoid being floating
8/20	19,25	Separate battery's SCL/SDA from EC_I2C2 bus:(a) BATT_SDA to EC pin PC4 (b) BATT_SCL to EC pin PA5 (c) 4.7kOhm pull-up resistors are required
8/20	25	Move R91200 to make sure PPVAR_SYS power consumption is readable via INA, in battery-only condition
8/20	19	Change R90880 back to 2.2k ohm. (refer to the comment of #14)
8/20	25,29	About PPVAR_USB_C0_VBUS, please reserve the following circuitry for experiment.
8/20	31	Add a 1kOhm series res from J17.16 to LID_OPEN
8/22	16	Add 0 ohm NC connects Q708 pin 1 to Q709 pin1. Add 0 ohm NC connects to Q707 pin1 to Q710 pin1
8/22	16, 24	Reserve U2001 XO_CEL pin 0 ohm NC connects to ANX7625 XTAL_OUT(C1 pin)
8/22	16	Add a 0ohm on ANX7625_XTAL_IN in case XTAL drive level needs to be tuned
8/22	16	ANX7625_INT_L -> MIPIBRDG_INT_ODL
8/22	8	Connect MIPIBRDG_INT_ODL to AP pin AC3
8/22	16	Pull-up R91238 to PP1800_AP instead of PP1800_MIPIBRDG_D
8/22	16	[Netname] (a) J15.13: PP3300_CAM (b) PP1800_MIPIBRDG_EN -> EN_PP1800_MIPIBRDG
8/22	7,16	Connect EN_PP1800_MIPIBRDG_DX to AP pin AE25 (GPIO36)
8/22	16	Reserve 0ohms bypassing Q708/Q709 and Q707/Q710
8/22	16	Reserve a testpoint on ANX7625 CABLE_DET for debug usage
8/22	16,21	Reserve power path from VCAMIO_PMU to PP1800_MIPIBRDG
8/22	16	Move C10525 to PP3300_EDP_DX, close to eDP connector
8/22	16	Fix note of R252: "TODO: VALIDATION OF SHARING POWER BETWEEN BRIDGE AND EDP PANEL"
8/22	16,21	Reserve power path from VMCH_PMU to PP3300_MIPIBRDG_DX
8/27	32	Add note to GMR sensor: "DNS IF GMR IS ON SUB-BOARD"
8/27	4,26	Change U6570 to RT6256C and U6571 to RT6256B to improve power consumptoin. Update power tree
8/27	28	[OEM] Remove keyboard backlight circuit
8/27	34	Change ac coupling capacitors to follow it6505fn_v35_20190722.pdf (need to verifiy on proto board)
8/29	19,26,30,32 35	[For G3 power consumption] (a) Add LDO for powering PP1800_EC and PP1800_H1, input from PP3300_ALW. Netname PP1800_LDO (c) Change R90987 to 100kOhm, and reconnect U6554 EN pin to PP3300_SERVO_INA with R90987 (d) Change R91148 to 1MOhm (e) Reconnect PP1800_ALW_PG to PP1800_H1_PG (f) Modify H1_RST_ODL circuit as shown in note (g) Change R91196 to 100kOhm, still DNS'd (h) Add control circuit from EC PA14 via a 0ohm to U6569 EN, a mosfet inverter is needed as EC cannot take PPVAR_SYS voltage. Netname EN_PP1800_S5_L
8/29	25	Add a PMOS back-to-back with Q789 to avoid negative power source going into ISL9238C ADP pin, whose AMR minimux is -0.3V
8/29	26	Add a 0 ohm between EC PA14 and EN_PP1800_S5_L. Populate this resistor by default.
8/29	26	Reserve 1M ohm (DNS by default) between LDO3_VOUT and the EN pin of RT6256CGQUF.
8/29	19	Add a 499k ohm between LID_OPEN and PP1800_EC. (To allow system bootup without GMR)
8/29	8	Please reserve a serial 0ohm on MIPIBRDG_INT_ODL.
8/29	34	[ITE suggestion] (a) DP_AUX_N reserve P/D 300K ohm (b) Change C10652,C10653 to 0.68uF (c) Add 100K P/D between IT5204 CTX/CRX and AC caps (d) Add serial 0ohm on USB_C0_SBU1_MUX/USB_C0_SBU2_MUX (e) Add serial 22ohm on EC_I2C_USB_C0_MUX_SCL/SDA
8/30	19,29,30	Some PP1800_ALW should be changed to PP1800_LDO or PP1800_EC - Q739A.5 (PP1800_EC) - R619 (PP1800_EC) - R338 (PP1800_EC)
8/30	8	Nit: remove note for MDSI_TE "NEAR CON9102"
8/30	29	For better ESD protectoin and filtering, move ESD7102, C518, and C10637 to be closet to USB-C connector.
9/2	19	Stuff R90868
9/10	19	Change BOARD REV ID from 0 to 1
11/4	25	Having 0 ohm to bypass Q801 for cost saving, since it's for reverse plugging protection
11/4	19	It's better to add and populate 0 ohm by default between. - EC_I2C2_3V3_SCL and BATT_SCL_3V3, - EC_I2C2_3V3_SDA and BATT_SDA_3V3
11/4	34	Please refer to it6505fn_v36_20190903.pdf (Add R91298)
11/4	21	Add a 0 ohm (populate by default) between DVDD18_TO (U2001.L9) and VIO18_MT6358 and de-populate R90656.
11/4	33	Change R91181 (LID_OPEN) back to 0 ohm
11/4	12	Please add resistor of 0 ohm on USB2_DM and USB2_DP. (For USB SI measurement)
11/4	12	Change R90741 from 680 ohm to 619 ohm for USB2.0 S/I
11/4	2	Update EC I2C MAP for bigbang
11/4	29	Netname nit: BC12_POGO_ADDR -> BC12_C0_ADDR, BC12_POGO_EN_L -> BC12_C0_EN_L
11/7	19,25	Change ISL9238CHRT2-T's I2C to EC_I2C2_3V3_SDA from BATT_SDA_3V3 ; to EC_I2C2_3V3_SCL from BATT_SCL_3V3

